Investigation of Integrated Circuits For High Datarate Optical Links

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Investigation of Integrated Circuits for High Datarate Optical Links

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This is dedicated to my family and loved ones

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SUMMARY

Because of the need to move large amounts of data efficiently, optical based communications are a critical component of modern telecommunications. And as a key enabler of optical communications, electrical components play a critical role in optical data links. Optoelectronic integrated circuits provide the bridge between the optical and electrical realms. Electronic integrated circuits are also integral parts of the optical link, interfacing with post processing circuitry and compensating for any limitations along the link. In this investigation, three circuits for optical data link applications are studied. The circuits consist of two optoelectronic integrated circuit front-ends for freespace and long haul applications, respectively, and an active filter for near end cross talk cancellation associated with high data rate transmission.

CHAPTER 1

INTRODUCTION

Optical communications are a critical component of today's telecommunications network. The applications of optical communications span a wide from long haul communications that stretch across oceans to routing of backplane signals to board to board interconnects that only stretch a few centimeters. The drive to optimize optical communications is the enormous traffic of voice, electronic, and data communications. The demand continues to increase and shows no sign of an end in sight.

The frequency of light is many orders of magnitude greater than electrical signals. This gives a bandwidth that nears the terahertz regime rather than gigahertz for electrical systems. The increased bandwidth provides higher capacity for data transfer enabling quicker transfer of more data. This data takes the form of extremely high-speed digital signals. However because all the data processing is done in the electrical realm, the data must eventually be converted into electrical signals. A representative diagram of an optical transmission system where optoelectronic integrated circuits (OEICs) may be used is shown in Figure 1.1. Multiple data streams are combined together with some sort of multiplexing. This digital data, which may be first processed, is then converted to an optical signal by driving some sort of laser. The optical signal is transmitted through a medium, which may be waveguides, fiber, or freespace, to the receiver. The receiver consists of a photodetector which converts the optical signal back to electrical so that an

amplifier can pass the signal to subsequent processing circuitry. Finally the data is recovered and demultiplexed and then distributed. Optoelectronics form the union between the optical and electrical components. The primary role of optoelectronic circuits is to translate information between the optical domain and the electrical domain.

Optoelectronic circuits are a natural development of the evolution of both integrated optics and electronic integrated circuits, leveraging the optical components to implement a high-bandwidth medium for data that can be processed by the electronics components. Combined optical and electrical circuits take two different forms: photonic integrated circuits (PIC) or optoelectronic integrated circuits (OEIC) [1]. The PIC is comprised of several optical components integrated with a few transistors. An OEIC describes a monolithic integrated circuit combined with a few optical components. The need for optoelectronics is spurred by the benefits of transmitting data through optical rather than electrical signals. Transmission bandwidth in optical fiber can achieve 10 Tbits/s, easily surpassing that of copper-based cables traditionally used in telecommunications. Optical signals can also overcome many other limitations of high-density and high-speed electrical interconnects such as coupling and RC time constants. The electrical components of the system provide ease of processing the signal such as amplification and noise cancellation.

The objective of the proposed research is to investigate microwave monolithic integrated circuit (MMIC) topologies that can be applied to the needs of optical interconnect applications. As a key enabler of optical technology, electrical components play a critical role in optical data links. Optoelectronic integrated circuits provide the bridge between the optical and the electrical realms. Electronic integrated circuits are

integral parts of the optical link, interfacing them with post processing circuitry and compensating for any limitations along the link. In this investigation, three circuits for optical data link applications are studied. Two optoelectronic front-ends for freespace and long haul applications, respectively, and an active filter for near end crosstalk cancellation associated with high data rate transmission. The first application is a highly compact low-power receiver for board-to-board interconnects. The second application is a wide bandwidth, low-cost receiver at the 1.55μm wavelength for high data rate long-haul telecommunications. The third application is an analog CMOS filter that emulates crosstalk noise in backplane routing applications.

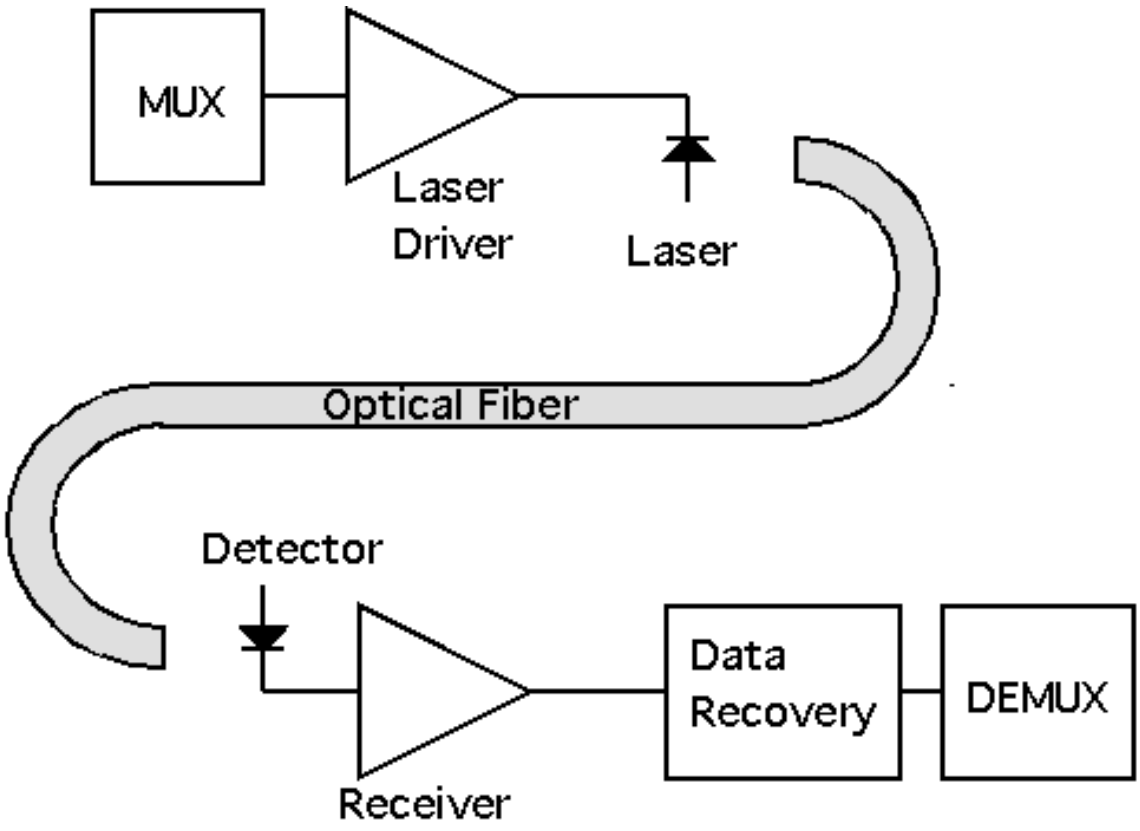


Figure 1.1 Typical Optical Transmission System

Free-Space Optical Interconnects

An application of optical communications is board-to-board optical interconnects. These systems are characterized by many parallel channels at lower data rates, typically in the MB/s, and short distances measurable in centimeters, typically without the benefit of fiber connection.

Figure 1.2 shows a general diagram of a free-space optical link. The link would provide a bus between closely spaced boards. Arrays of lasers and detectors provide a means for massively paralleled data transfer, thereby bypassing the difficulties of implementing electrical buses. The alignment between the transmit and receive sections is improved through the use of fiber bundles, microlenses, or even miniature servos to focus and help direct the optical signal.

At the board level, optical interconnects can bypass several limitations faced by electrical buses. At high-speed operation, clock skew occurs when the same state of the timing signal reaches various components at different times, thereby preventing synchronous operation between several components in a system. The routing path, cross talk, and the finite speed of the electrical signal introduce delays. The RC time constants formed by the parasitic capacitance and resistance of the electrical board interconnect become problematic above several hundred MHz and limit circuit performance. The high concentration of signal lines risk interference from radiation and coupling between closely spaced lines.

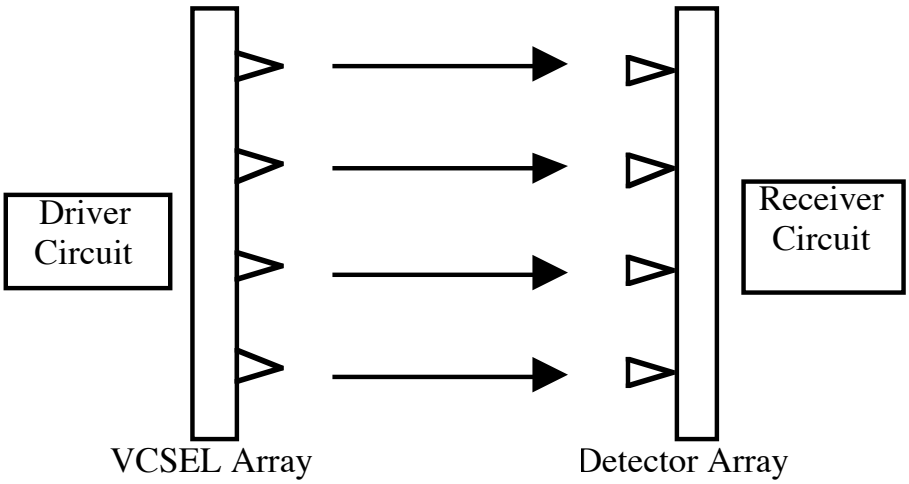


Figure 1.2 Free-Space Optical Interconnect

Free-space interconnects grant greater flexibility in routing signals, removing the need for hard-wired connectors. Optical signals are routed with the speed of light and are immune to capacitive loading effects, which help eliminate the problem of clock skew. There are no mutual interference effects between optical signals that cross or propagate together. Large fanouts can be accommodated with a lower system power requirement. Board-to-board interconnects demand low-power circuits because multiple receivers are used in arrays. The challenge in these designs is to achieve low-power operation with enough output drive capability to transmit the signal to the subsequent processing components which are typically implemented in CMOS,

The primary thrust of current research in free-space board-to-board interconnects is in design of the optical source, the vertical cavity surface emitting laser (VCSEL), improving transmission of the optical signal, and on-system design of the transmission system [14-15]. Although the major obstacles in realizing board-to-board interconnects

are not due to limitations in electronics, there are real challenges in circuit design to realizing a low-cost, low-power array of receivers. Designs suited for long distance communication often are too expensive or too power consuming.

For free-space optical interconnects, a robust system can be realized only with efficient arrays that can handle highly paralleled optical input and output. Demonstrations of working free-space interconnects have been implemented with hybrid designs, separating the optical and electrical components [14-15]. The advantage of monolithic design is the potential for very compact arrays with highly repeatable manufacturing tolerances. One of the main problems with the receivers fabricated monolithically for the free-space interconnects is that they have been implemented in low-yield or experimental processes [16-17].

High Data Rate Long Wavelength Receivers

In the past, the optical and electrical components were separated and individually packaged before being assembled. Although this isolated the packaging requirements of the two different types of components, the tradeoff was assembly complexity and lower yields that resulted from such complex processes. As the trend towards higher integration progresses, new packaging techniques need to be developed to accommodate the demands of both electrical and optical packages.

The influence of packaging upon optoelectronic integrated circuit performance is significant. Variations in input capacitance as small as 50 fF can cause significant shifts in receiver performance [1]. The tight tolerances necessary for mating optical connections comprises a significant portion of the cost of optoelectronic components.

Increasing the amount of acceptable misalignment between the optical signal and the detector can reduce cost by easing manufacturing requirements. Another determinant of optical component cost is the material system used to fabricate the component. The InP-based material system allows use of the longer wavelengths 1.3 μm and 1.5 μm, which enables low-loss, low-dispersion fiber communications, but the fabrication costs are more expensive and do not offer electronics that are as mature as other material systems like silicon or gallium arsenide. For integrated high-speed components, the margin afforded by low parasitic, alignment-tolerant packaging, and lower material costs can maximize the cost performance of a component.

The rapidly increasing demand for data is driving the need for high data rate networks. In the near future, current systems will not be able to provide the level of performance required and in response, new standards have been defined for 40 GB/s and higher data rates. High-speed photoreceiver front-ends for long wavelength systems are expected to play a major role in these telecommunication systems. To handle these data rates, high-frequency designs with broad bandwidths are needed to accommodate the digital signals. Several circuit topologies have been successfully used for front-end amplifiers with bandwidths in the tens of GHz. The transimpedance topology is a familiar and popular single-stage design used in optoelectronic receivers. Another design used more recently to implement the wider bandwidth designs is the distributed amplifier.

There has been extensive research into implementating photoreceivers for data rates in the 10-20 GB/s range. Typically these circuits are made up of InP-based circuits. The devices of choice are high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs). The InP-based material system is favored for long

wavelength high-speed OEICs because of the high-performance photodetectors and the excellent high-frequency performance of transistors fabricated in the high-mobility material system. This allows a monolithic implementation that reduces packaging parasitics that become problematic at high frequencies.

The most commonly used circuit has been the transimpedance (TZ) amplifier. The transimpedance amplifier converts current to voltage, showing better dynamic range and sensitivity trade-offs compared with other current to voltage conversion circuits [2]. The advantages of the transimpedance amplifier are its compact size and simplicity. Transimpedance topologies have been used in 10-20 GB/s OEICs with HEMTs [3], and HBTs [4-5]

Not all long wavelength OEICs require the electronics to be fabricated in InP-based material systems. From the circuit perspective, it is more desirable to utilize a more mature electronics material system such as GaAs. One of the more exotic methods used to monolithically integrate receiver front-ends with long wavelength detectors is InP on GaAs heteroepitaxy. The first OEIC in the GHz range made in this manner was demonstrated by Y. Mihashi, et al. [6]. The challenge of this method is minimizing the defects that arise from growing mismatched layers. These defects can propagate through the optical layers and severely degrade photodetector performance. To minimize these problems, buffer layers are grown between the optical and electrical layers. Higher data rate receivers have recently been fabricated in this method, demonstrating operation in the 10-20 GB/s regime [7-8].

As the data rates climb above 10 GB/s, the conventional transimpedance topology becomes less suitable because of the degraded signal to noise ratio and the need for

transistor cut-off frequencies at least an octave above the maximum frequency of operation [9]. The distributed amplifier is well suited for very wide bandwidth designs that are necessary to implement data rates above several tens of GB/s [10-12]. The distributed amplifier, also known as the travellingwave amplifier, allows for bandwidths that approach the cut-off frequency of the transistors and allows the use of commercially available MESFETs for 20-40 GB/s systems [13].

Crosstalk Cancellation

Once the optical data is translated into electrical signals, the data faces further challenges from high speeds due to imperfections in the electrical realm. As electrical components gradually improve to take advantage of optical high speed advantages, implementation will be a combination of the two extremes outlined earlier, with high data throughput maximized with a combination of high speed circuitry and parallel electrical channels. An example system is shown in Figure 1.3 where an optical unit transfers data from fiber to a PC backplane. However, routing more than one channel on boards suffers from the possibility of signals interfering with each other. This bottleneck becomes apparent when routing from optical daughter cards onto backplane channels.

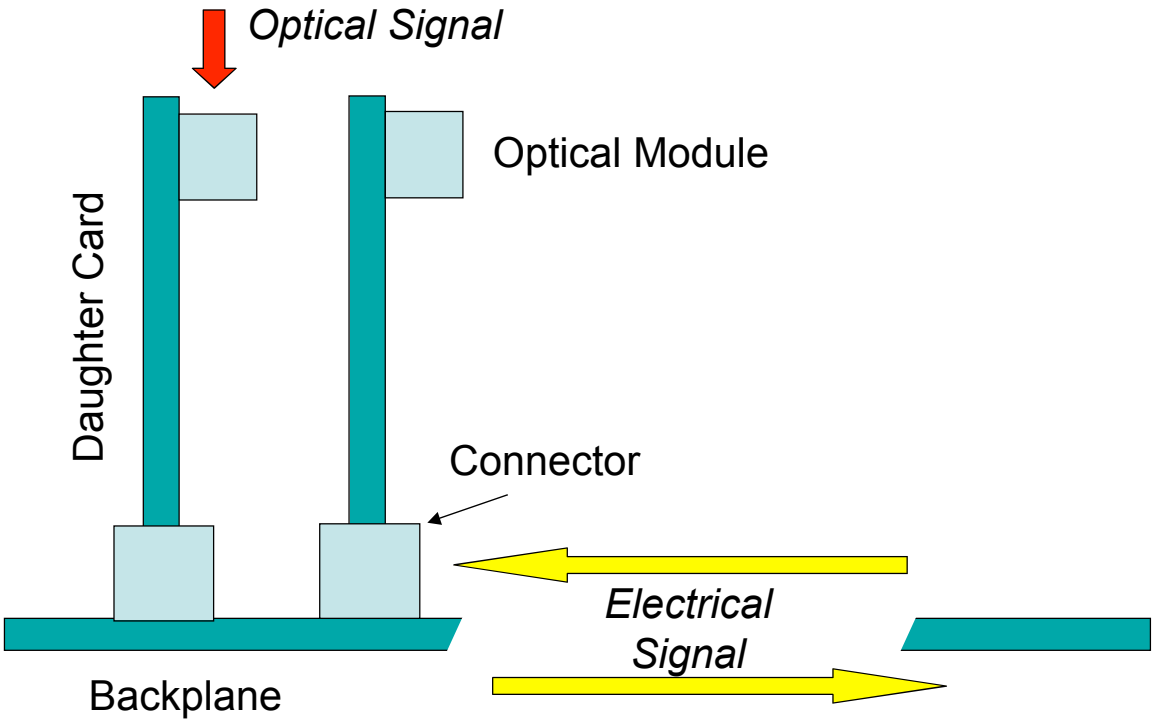


Figure 1.3 Optical Daughter Card in Backplane

The need to route the increasing amounts of data traffic has made the backplane a bottleneck in networking infrastructure. Advances in optical links and supporting electronics have increased the speed and amount of data streams handled by a system. Backplanes comprise the physical highway and infrastructure for this data transmission and are often entrenched and difficult to change without great effort and trouble. As a result, legacy backplanes are not keeping pace with other technical improvements for delivery of multi-gigabit serial data traffic and are becoming a critical bottleneck.

High-speed data transmission across backplane channels suffers from multiple sources of impairment. The channel is intrinsically dispersive and noise from adjacent channels leaking from connectors corrupts the desired signal [18-20]. Equalization can compensate for the low pass response of the forward channel but this aggravates the

problem of cross-talk (XT) noise. Coupling of adjacent signals through adjacent pins in backplane connectors generates cross-talk noise that becomes more problematic at higher frequencies. Equalizing the received signal boosts the high frequency components of both the transmitted signal and cross-talk noise, thereby canceling any benefits from equalization. Cross-talk noise can be divided into Near End Cross-Talk (NEXT) and Far End Cross-Talk (FEXT). NEXT noise is of a much higher magnitude than FEXT noise because of its closer proximity to the receiver and has been identified as the major impediment to speed performance above 5Gps [19], [20].

CHAPTER 2

8X8 SDM RECEIVER ARRAY

Background

One application for optical interconnects is to overcome limits in conventional electrical interconnects. For example, current personal computers have internal buses that route data on the order of tens of gigabytes per second. As processor speeds steadily improve, requirements for higher data throughput is necessary. Maintaining signal integrity at the higher datarates is a serious design challenge. One means to overcome limitations in electrical interconnects is to utilize optical interconnects. A spatial domain multiplexing (SDM) chipset provides increased capacity through highly paralleled optical interconnects.

Most research into paralleled spatial arrays have focused upon free-space optical interconnects. The thrust of previous research in free-space board-to-board interconnects have been in design of the optical source, the vertical cavity surface emitting laser (VCSEL), improving transmission of the optical signal, and on-system design of the transmission system [14-15]. Although the major obstacles in realizing board-to-board interconnects are not due to limitations in electronics, there are real challenges in circuit design to realizing a low-cost, low-power array of receivers for optical communication.

For free-space optical interconnects, a robust system can be realized only with efficient arrays that can handle highly paralleled optical input and output.

Demonstrations of working free-space interconnects have been implemented with hybrid designs, separating optical and electrical components [14-15]. The advantage of monolithic design is the potential for very compact arrays with highly repeatable manufacturing tolerances. One of the main problems with previous work in free-space optical interconnects is the implementation in low-yield or experimental processes [16-17].

Spatial Division Multiplexing

The concept of spatial division multiplexing is illustrated in Figure 2.1. Two example implementations of an optical SDM link are shown in Figure 2.2. A simple optical SDM data link can be formed by imaging an array of light emitters onto an array of photoreceivers. Each emitter photoreceiver pair forms an independent optical channel. These optical channels paralleled together form the multiplexed signal. The primary limitation of these channels is the need to maintain a coherent optical signal usually done with an imaging optical channel. This requirement makes SDM best suited for short link distance for applications such as chip-to-chip or board-to-board interconnection needs.

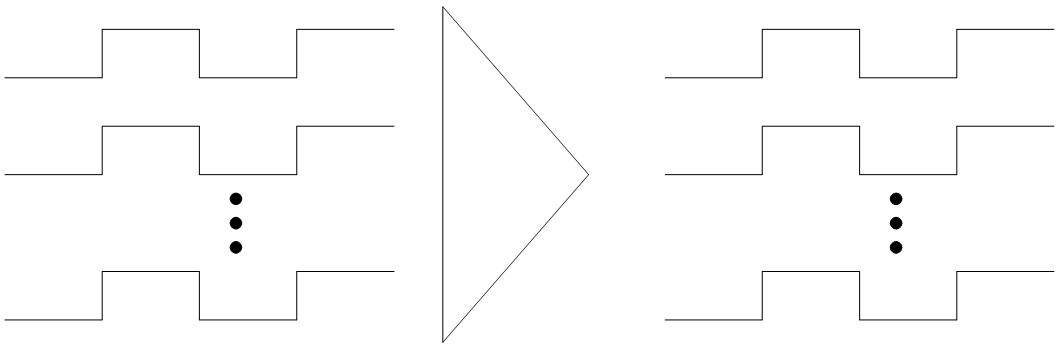


Figure 2.1 Spatial Division Multiplexing Diagram

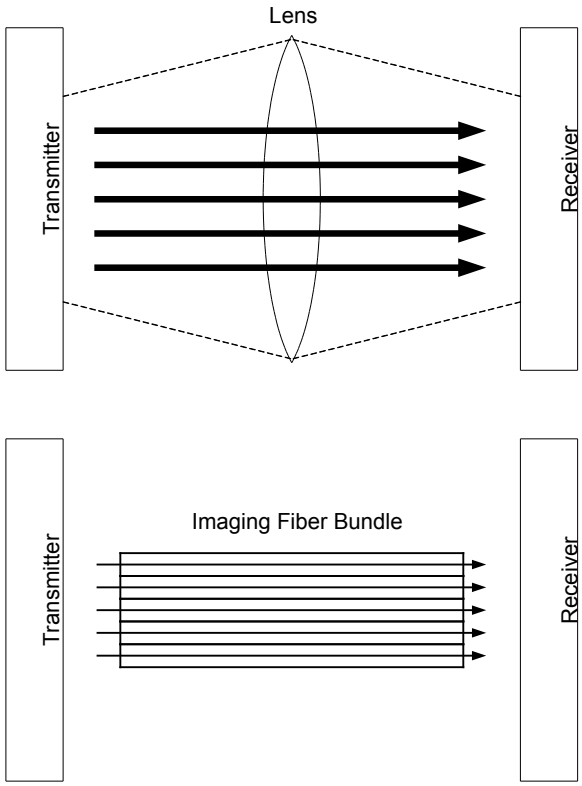


Figure 2.2 Typical Spatial Division Multiplexing (a) via Free Space (b) via Imaging Fiber Bundle

SDM achieves high data rate transmission via paralleling several low speed data streams in either the electrical or optical realm. In an optical SDM system, individual channels are physically separated from each other and arranged as arrays of lasers and detectors aligned together. When optical imaging is achieved, each light emitter and corresponding photoreceiver forms an independent optical channel. The optical data is passed along multiple independent optical channels in parallel. Therefore, data streams on each light emitter-receiver pair are spatially multiplexed down the optical channel. A simple SDM data link can be formed by using a relay lens that images an array of light emitters on an array of photoreceivers or even transmit through free-space provided the

arrays are close enough. SDM can be compared to conventional time division multiplexing (TDM) and wavelength division multiplexing (WDM), which use time and wavelength, respectively, to multiplex data streams down a single optical channel. In the optical realm, there are several such techniques such as wavelength division multiplexing (WDM) or spatial division multiplexing (SDM). Both techniques pass multiple streams separated from each other.

Time Division Multiplexing

Time division multiplexing adds several low datarate streams into a single high datarate stream. The technique is illustrated in Figure 2.3. The difficulty of this technique is that to multiplex more and more streams, the circuitry must be capable of higher and higher speed operation. The operating speed of the electronics limits the overall capacity of the link. At very high datarates, limitations in sending data through fiber also conspire to degrade overall signal integrity. Routing high speed optical signals through long distance through fiber require a means to counteract the effects of dispersion in the fiber.

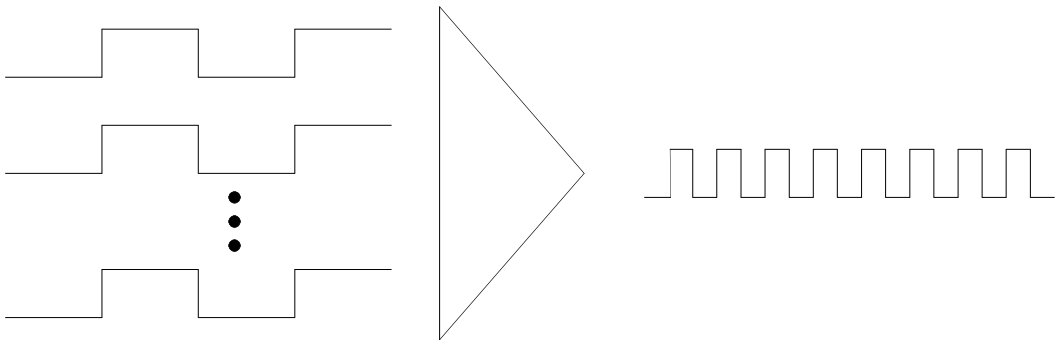


Figure 2.3 Time Division Multiplexing Diagram

Wave Division Multiplexing

Wave division multiplexing is effectively the same principle frequency division multiplexing used in radio and wireless systems. Data is transmitted simultaneously at multiple carrier wavelengths over a fiber. Figure 2.4 shows the concept of WDM. To the first order, interference between different wavelengths is minimal if properly spaced. To utilize WDM, higher performance components are required to be able to transmit, carry, and receive signals from multiple wavelengths. For interexchange, enterprise networks, and long haul links, the increased capacity makes up for the complexity required. The capability to transmit lower datarate signals reduces the effect of dispersion in the fiber, thereby reducing the number of required repeater or booster amplifiers for long distances. However, the more stringent requirements of WDM systems and the complications of having to deal with multiple wavelengths make it less suitable for short haul applications.

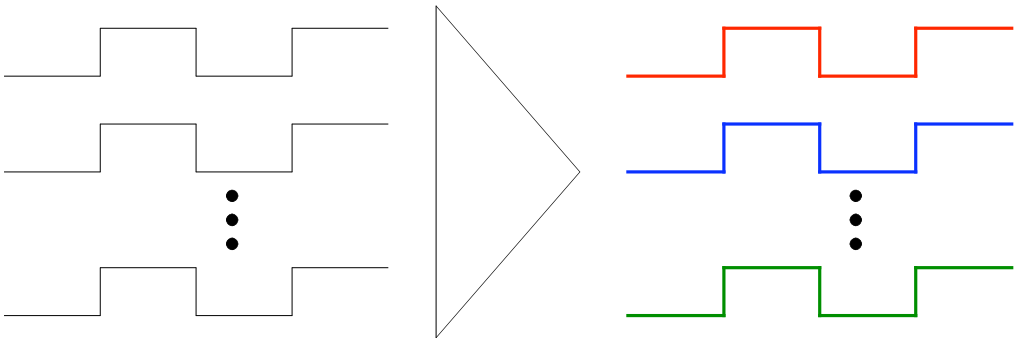


Figure 2.4 Wave Division Multiplexing Diagram

Optical SDM is well suited to short link distances for applications such as chip-to-chip or board-to-board interconnection needs where transmitter and receiver can be either

aligned for free space transmission or the data routed with some sort of imaging optical channel. The imaging optical channel can be a lens or imaging fiber bundle. The SDM system achieves high data throughput via massively paralleled channels. The quantity of optical channels requires an equal quantity of low power electronic circuits to translate the optical signals to a usable electrical form. SDM offers simplified interface electronics due to lower channel data rates as compared to TDM approaches. The optical SDM channel only deals with a single wavelength and therefore requires simpler optics compared to WDM approaches. SDM has distinct advantage over TDM for short interconnects in cost and power because of its simplicity.

Spatial Division Multiplexing Array Link

Figure 2.5 diagrams the SDM demonstration array. A laser driver circuit modulates a VCESEL within an 8x8 VCSEL array. An 8x8 array of photoreceivers captures the optical signal and drives standard CMOS circuitry. In this research, the laser driver and amplifier for the receiver are fabricated in a commercial foundry process. The VCSELs are fabricated separately in a metal organic vapor phase epitaxy (MOVPE) process. However, the photodetector array is monolithically integrated with the amplifier using a non optimized photodetector structure. The design target is to demonstrate the possibility of a link to form an aggregate data throughput of 64 Gb/s using 64 channels running at 1 Gb/s.

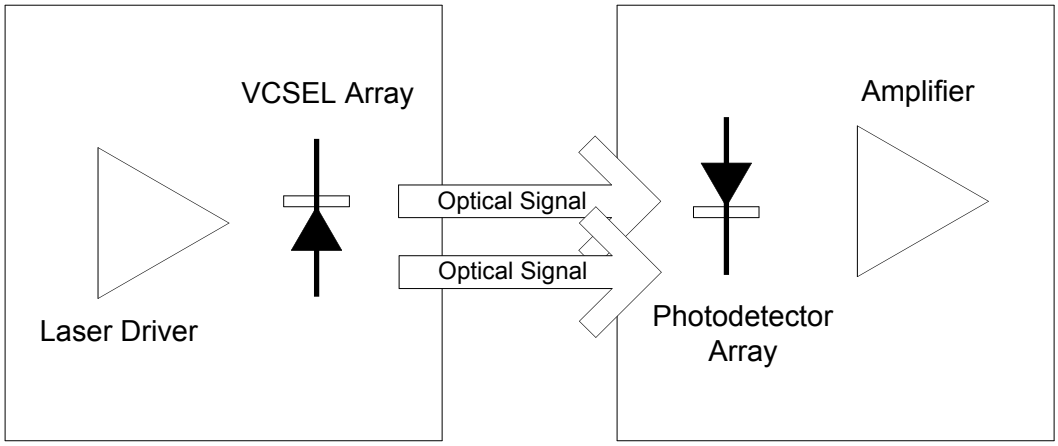


Figure 2.5 Optical SDM Link Array

Transmitter

Vertical Cavity Surface Emitting Lasers (VCSELs) enable high density optical interconnects because their structure is compatible with low-cost wafer scale fabrication and testing methods. The planar structure makes it much easier to form two-dimensional arrays unlike edge built light sources [21]. The VCSEL also has characteristics that make it well suited for fiber based optical interconnects. A circularly shaped output increases coupling efficiency to fiber. Low power consumption and high modulation bandwidths also make it very attractive for integrated optical links.

Semiconductor lasers are the most commonly used light source for optical communication systems. They are highly efficient in converting electrical energy to optical energy. Semiconductor lasers are compact and are readily fabricated with integrated semiconductor technology. In a VCSEL, different epitaxial layers are used to form a pair of reflective surfaces as shown in Figure 2.6. Generated light oscillates within the cavity and any transmitted waves out of the cavity will add in phase. The reflective surfaces sandwich a gain medium allowing the laser to generate a coherent

output when excited with enough energy. In a VCSEL, the gain layer is very thin with the reflective surfaces formed on the top and bottom surfaces of the semiconductor. Because the reflective surfaces are formed stacked on top of the substrate it allows VCSELs to be formed in 2D arrays.

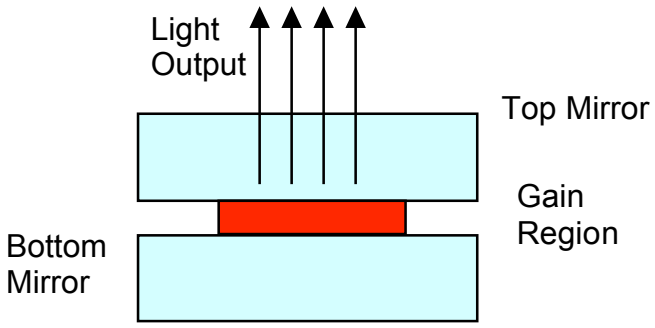


Figure 2.6 Structure of a Vertical Cavity Surface Emitting Laser

VCSELs can be fabricated into arrays of high performance light emitters and therefore are ideally suited for high throughput SDM links. VCSELs can be repeated in array with excellent uniformity. VCSEL arrays have shown less than 3% output power variation over 64 elements [22].

The VCSEL array for this research was fabricated in Sandia National Laboratories. The VCSELs are laid out in an 8x8 array as shown in Figure 2.7. A large spacing is used to mitigate the optical crosstalk from one channel to the other. The lasers are spaced at a 250 μm pitch and are approximately 15μm in diameter. Shown in Figure 2.8 is the measured performance of a single VCSEL with greater than 10% at several milliwatts of power levels [22]. When driven with GTL logic level, the VCSEL can be switched from a 2.5 mW power level to below 0.5 mW at various bias levels as shown in Figure 2.9.

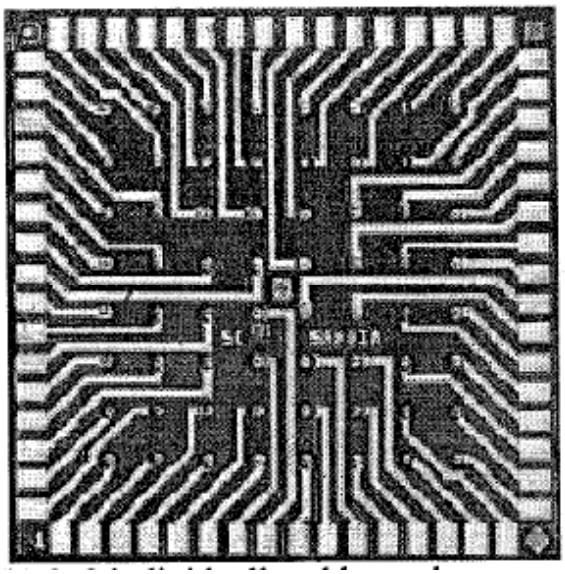


Figure 2.7 Photograph of 8x8 VCSEL Array

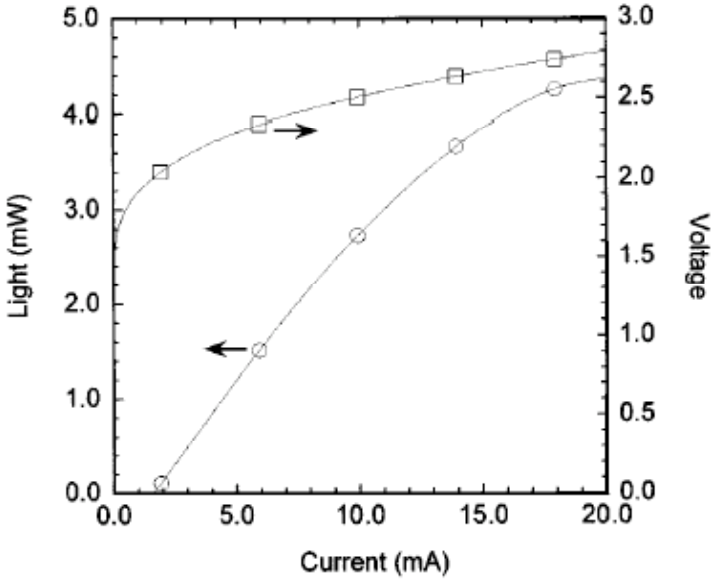


Figure 2.8 Measured VCSEL Performance

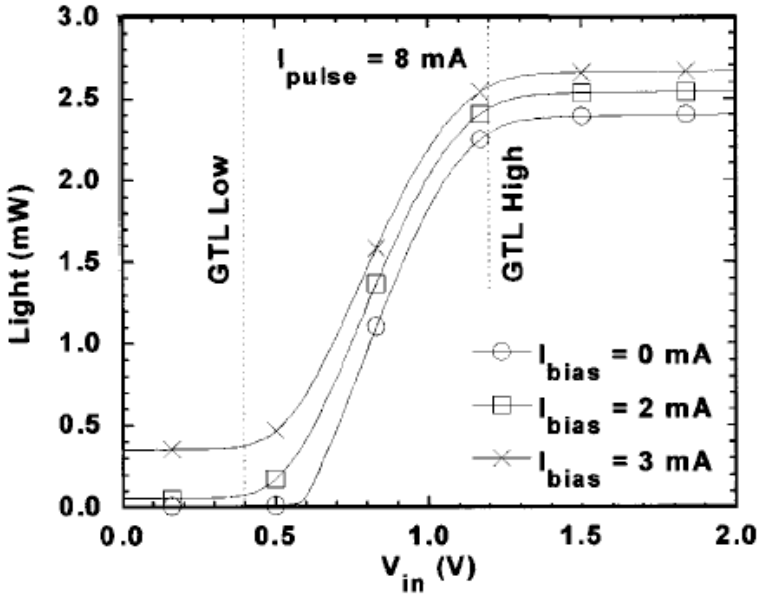


Figure 2.9 VCSEL Output at Various Bias Conditions.

VCSEL Array Driver Design Background

To drive the 8x8 VCSEL array, specialized 16-channel driver arrays (4 used per VCSEL array) were developed. Since the VCSELs' "on" voltage is about 2.5 V and can be even somewhat higher depending on a given VCSELs series resistance, a 5 V supply was selected in order to assure adequate circuit headroom. In order to be consistent with the receiver design discussed below, the drivers' inputs use gunning transceiver logic (GTL) levels.

A schematic for the driver of a single channel is shown in Figure 2.10. Each individual driver is comprised of two current sources (one for pre–bias and the other for the pulse current) and a differential switch. The current sources are made from enhancement-mode MESFET based current mirrors. The enhancement mode devices allow the driver to operate from a single supply voltage. Although the depletion mode

devices in this MESFET process generally have better speed and other operating characteristics, a current source designed with depletion mode devices would require a negative supply. The current sources from all 16 channels are controlled by two current injection inputs. The switch was made from large depletion-mode MESFETs. The FET sizes were optimized to maximize small-signal gain while maintaining a reasonable switching speed. After simulation and optimization, the gate size of 16 x 50 μm was chosen. The series connected diode connected transistors on the "dump" side of the switch are used to "look" electrically similar to the VCSEL. This improves switching symmetry and speed. Simulations demonstrate circuit operation to 5Gb/s.

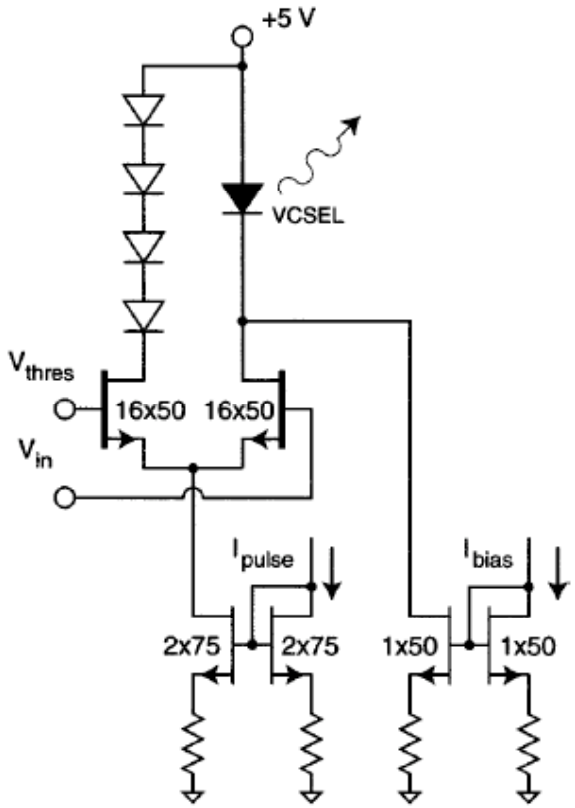


Figure 2.10 Schematic of Laser Driver Circuit

Photoreceiver Array

To achieve the high datarates, many paralleled channels are used in SDM links. With multiple channels, power dissipation becomes a primary concern for large arrays. A simple 8x8 array requires 64 transimpedance amplifiers. In order for the link to be practical, power dissipation needed to be kept below 2W. To obtain a low operating power, careful circuit scaling and GTL output buffers were used.

To minimize space and ensure maximum uniformity, the receive array for this SDM link requires a monolithic realization. Fabrication of amplifier circuitry on a process optimized for optical operation would have been wasteful. A process optimized for optical operation would have required epitaxial growths of layers that would not improve circuit operation. The photodetector requirements are not stringent and therefore photodetectors are fabricated in a conventional GaAs MESFET process.

The receive circuitry of the channel consists of the photodetector, transimpedance amplifier, decision circuit, and output buffer.

MSM Design

The photodetector is a critical component in optical communication systems. Semiconductor photodetectors absorb optical energy and generates an electron hole pair in the semiconductor material. When a voltage is applied, these electron hole pairs generate a current. Most often this is achieved by reverse biasing a diode junction in the semiconductor. There are many choices of photodetectors available to the designer. The choices can be divided into edge illuminated waveguide photodetectors and vertically

illuminated photodetectors. Optical signals are fed parallel to the substrate through the sides for edge illuminated photodetectors. Edge illuminated waveguide photodetectors include travellingwave photodetectors. Launching a signal from a fiber into a waveguide structure can be difficult to do without suffering significant coupling losses. In contrast, vertically illuminated photodetectors have the light incident perpendicular to the surface and generally more applicable for low loss fiber optical receivers.

The MSM detector is an example of one type of vertically illuminated photodetectors. Metal contacts form a diode connection to an optically reactive semiconductor. Incident light of the correct wavelength generate carriers which are collected by the metal contact fingers.

The photodetector chosen was a monolithic implementation of a metal semiconductor metal (MSM) photodiode. The MSM photodetector is easily fabricated with a GaAs and doesn't require special doping profiles. Conventionally engineered MSM diodes have several parameters including substrate structure and physical layout under control to influence the performance of the photodetector. The material system is engineered for absorption of incident optical power. By choosing the material system, the maximum absorption at a particular wavelength can be chosen. The efficiency of absorption of particular wavelengths depends on the bandgap of the particular material system. GaAs systems are better suited for short wavelength, ~850nm, absorption while material systems like InP and InGaP are better suited for long wavelength, ~1.5um, optical absorption.

The MSM photodiode is essentially a Shottky diode formed by a metal semiconductor contact. In the MESFET process, the gate metal forms this contact. An

interdigitated structure is used to increase responsivity by increasing the effective surface collection area. Figure 2.11 depicts a MSM photodiode. The speed of the MSM is determined by the carrier transit time between fingers and the RC time constant. The capacitance of the MSM also determines the speed because of the RC time constant involved. The capacitance can be estimated by using the following equation [23]

$$C_{pd} = \varepsilon_o(1+\varepsilon_r)\frac{\pi}{2\ln\left(2\sqrt{(1+\kappa')/(1-\kappa')}\right)}(N-1)S \tag{2.1}$$

$$\kappa' = 1-\tan^4\left(\frac{\pi}{4}\frac{W}{L+W}\right) \tag{2.2}$$

The resistance of the RC time constant of the detector is partially determined by the line resistance of the metal finger. The high resistance of very narrow and long collection fingers contributes to a large RC constant and slows the detector operation.

The dark current of the photodiode determines the sensitivity of the MSM at low optical power. Reduction of the dark current during design is critical for optoelectronic integrated circuit (OEIC) receivers with low detectable power. The dark current of a MSM photodiodes is caused by surface leakage current and from the bulk semiconductor. In GaAs material systems, the dark current from bulk material is relatively small and is typically ignored. Using passivation can reduce the surface leakage current. Typical dark currents for GaAs MSMs are in the nA range.

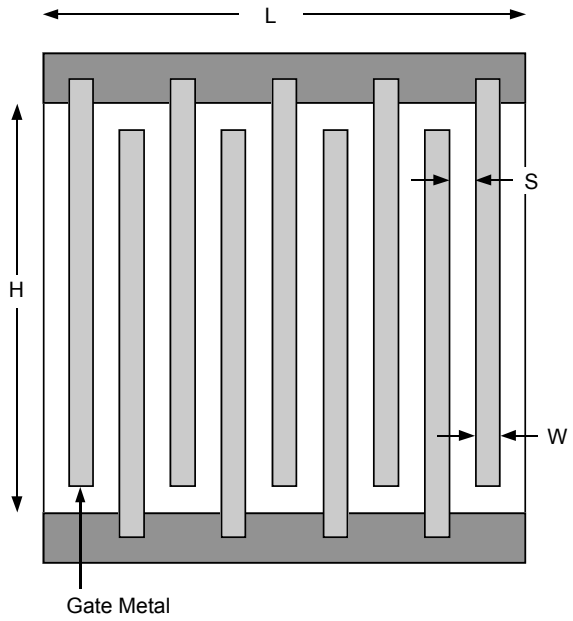


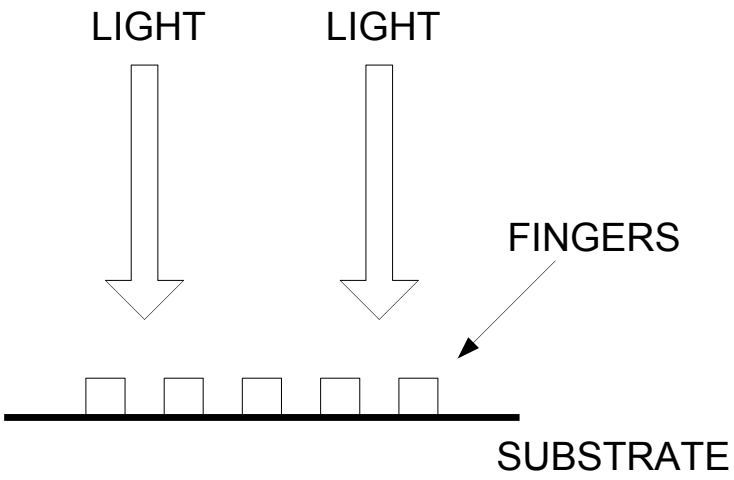
Figure 2.11 MSM Structure

In this project, a standard commercial MESFET process was selected for fabrication using a custom "parasitic" MSM photodetector. The gate metal of the MESFET process is used to form the contacts of the photodiode. There is no ion implantation under or between the contacts. This presents a less than ideal MSM detector due to slow hole transport in GaAs as well as less than optimal photo carrier collection. However, with high light levels available and relatively slow serial data rates, it is a sufficient solution to detect the optical signals.

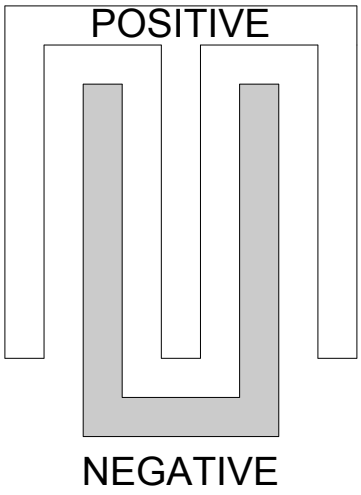
MSM Result

Because the optical properties of the process haven't been characterized, design of the MSM consisted of testing different finger dimensions to determine suitable performance. Figure 2.12 shows side and top profiles of the MSM photodetector.

Design of the MSM detector is accomplished by balancing the parameters of finger size and finger spacing for optimal efficiency and speed. Large finger widths will cover more area, thereby reducing the effective area available to collect optical energy. This reduction in useable optical area is referred to as metal shadowing. Narrow fingers will have increased resistance which slows the effective speed of the detector. Wide finger spacing will allow for more area exposed to the signal but the excited electrons will take longer to collect. At low voltages and widely spaced fingers, the generated carriers will take a significant amount of time before they are collected.



side view



top view

Figure 2.12 Top and Side Views of MSM Photodetector Structure

To find the optimal geometry of the MSM, various geometries were fabricated and tested. Table 2.1 shows the various geometries of MSMs fabricated and the calculated capacitance.

The devices were fabricated and measured . Some of the results for efficiency and responsivity are shown in Figures 2.13 and Figure 2.14.

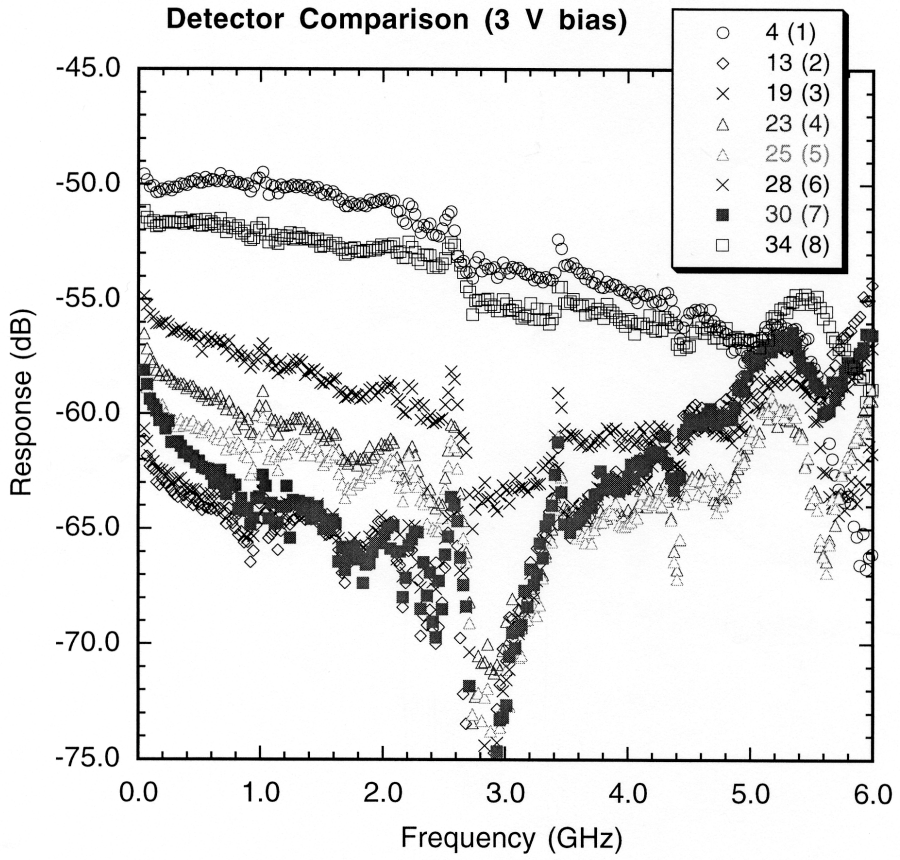


Figure 2.13 Comparison of MSM Responsivity

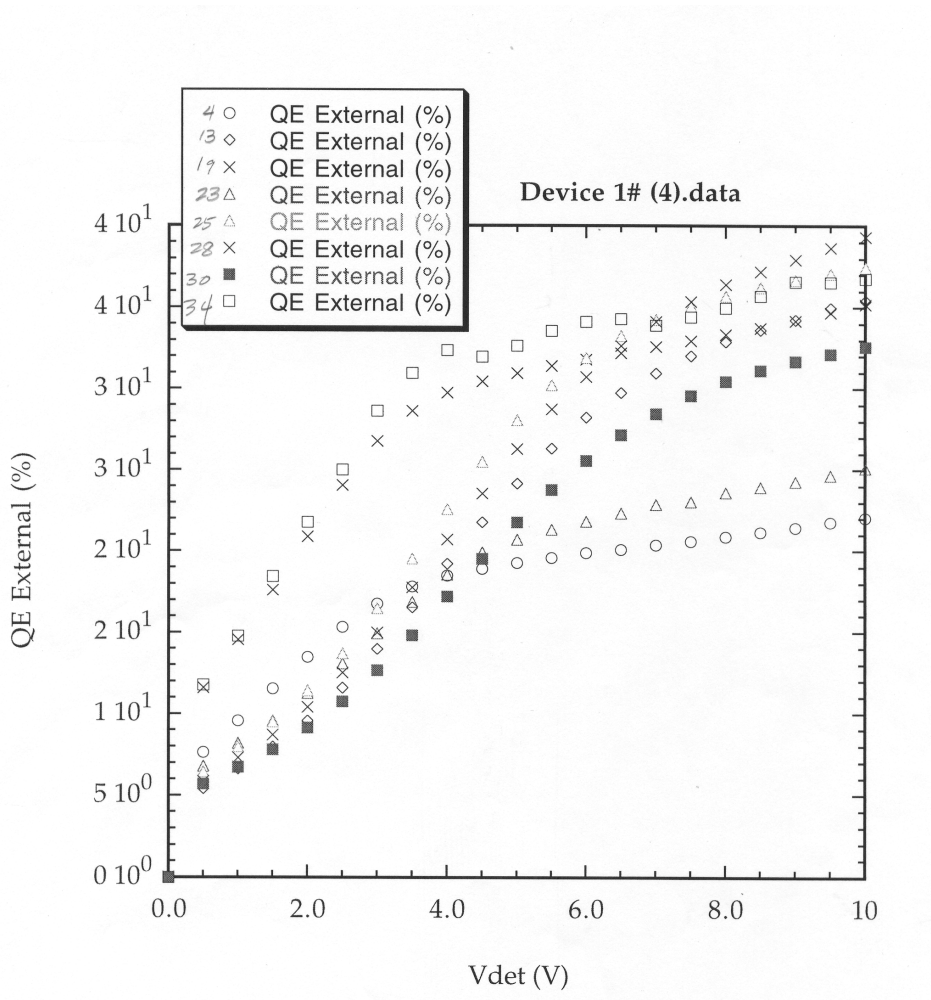


Figure 2.14 Comparison of MSM Quantum Efficiency

Table 2.1 Various MSM Geometries and Capacitances

MSM	Area	Spacing	Width	Fingers	Capacitance
1	50 μm^2	1 μm	1 μm	26	86.46 pF
2	50 μm^2	1 μm	2 μm	17	73.3 pF
3	50 μm^2	1 μm	3 μm	13	64.7 pF
4	50 μm^2	2 μm	1 μm	17	42.1 pF
5	50 μm^2	2 μm	2 μm	13	41.5 pF
6	50 μm^2	2 μm	3 μm	10	36.7 pF
7	50 μm^2	3 μm	1 μm	13	27.2 pF
8	50 μm^2	3 μm	2 μm	11	29.4 pF
9	50 μm^2	3 μm	3 μm	9	27.7 pF
10	50 μm^2	4 μm	1 μm	11	20.5 pF
11	50 μm^2	4 μm	2 μm	9	21.1 pF
12	50 μm^2	4 μm	3 μm	8	21.6 pF
13	50 μm^2	5 μm	1 μm	9	15.2 pF
14	50 μm^2	5 μm	2 μm	8	16.9 pF
15	50 μm^2	5 μm	3 μm	7	16.9 pF
16	75 μm^2	1 μm	1 μm	38	191.9 pF
17	75 μm^2	1 μm	2 μm	25	164.9 pF
18	75 μm^2	1 μm	3 μm	19	145.5 pF
19	75 μm^2	2 μm	1 μm	26	98.7 pF
20	75 μm^2	2 μm	2 μm	19	93.4 pF
21	75 μm^2	2 μm	3 μm	15	95.6 pF
22	75 μm^2	3 μm	1 μm	20	64.5 pF
23	75 μm^2	3 μm	2 μm	16	66.2 pF
24	75 μm^2	3 μm	3 μm	13	62.2 pF
25	75 μm^2	4 μm	1 μm	11	46 pF
26	75 μm^2	4 μm	2 μm	13	47.4 pF
27	75 μm^2	4 μm	3 μm	11	46.2 pF
28	75 μm^2	5 μm	1 μm	10	34.1 pF
29	75 μm^2	5 μm	2 μm	51	36.3 pF
30	75 μm^2	5 μm	3 μm	34	38.1 pF
31	100 μm^2	1 μm	1 μm	25	345.8 pF
32	100 μm^2	1 μm	2 μm	34	302.4 pF
33	100 μm^2	1 μm	3 μm	26	258.7 pF
34	100 μm^2	2 μm	1 μm	20	173.7 pF
35	100 μm^2	2 μm	2 μm	26	172.9 pF
36	100 μm^2	2 μm	3 μm	21	154.9 pF
37	100 μm^2	3 μm	1 μm	17	113.2 pF
38	100 μm^2	3 μm	2 μm	21	117.7 pF
39	100 μm^2	3 μm	3 μm	17	110.7 pF
40	100 μm^2	4 μm	1 μm	15	81.8 pF
41	100 μm^2	4 μm	2 μm	18	84.2 pF
42	100 μm^2	4 μm	3 μm	15	86.3 pF

Figure 2.15 shows the measured extrinsic quantum efficiency and responsivity of the chosen MSM photodetector design. A quantum efficiency of over 25% was obtained at 3V bias. Considering that the process isn't optimized for optical components, the efficiency is very acceptable. With milliwatt power available form the VCSELs, a 25% efficiency is adequate for proper operation. The small signal response of the detector is shown in Figure2.16 and was measured using a network analyzer. The 3dB bandwidth of the detector is above 2.5GHz. Measurements were constrained by limitations of the equipment.

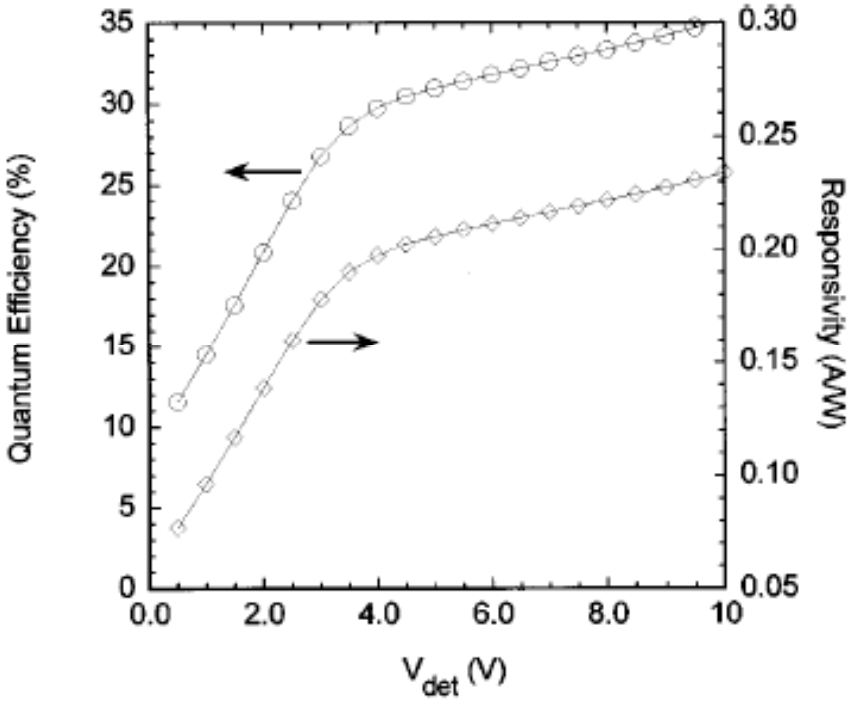


Figure 2.15 Extrinsic Quantum Efficiency and Responsivity of MSM 4

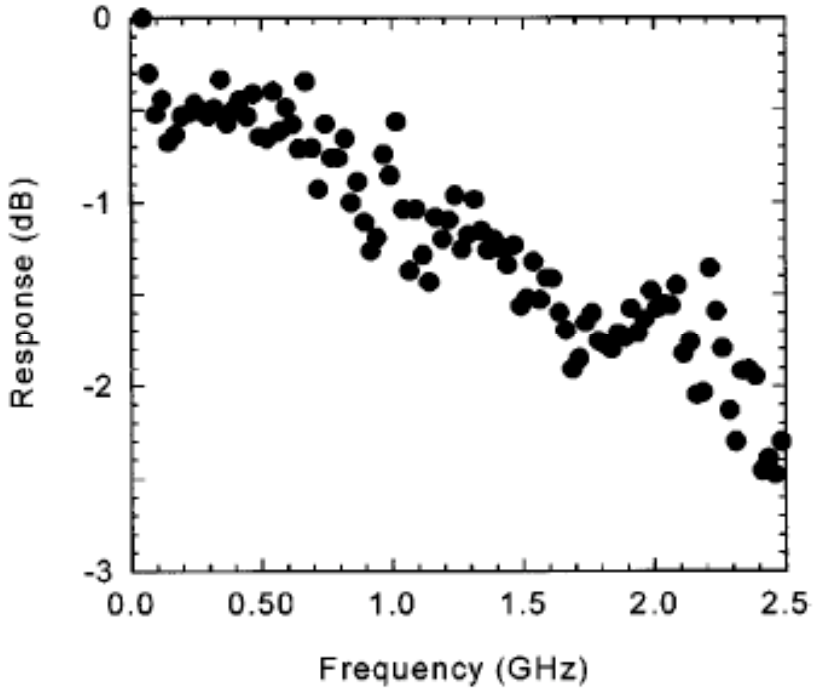


Figure 2.16 Small Signal Response of Detector

Transimpedance Amplifier Design

The most popular design for optoelectronic receivers is the transimpedance amplifier. A representative topology is shown in Figure 2.17. The amplifier represents a single stage design consisting of three sections. In the first section, there are two FETs in the common source configuration. The top FET acts as an active load, allowing a higher small signal resistance while maintaining a small voltage drop across the load. This gives an inverting gain section. The second section provides the voltage shift necessary for the feedback to work. The DC voltage level coming out of the first section is much higher than the DC voltage at the input of the amplifier and must be "dropped" through a unity gain stage. In the unity gain stage, there are several diodes shifting the DC voltage so that both ends of the feedback resistor are at approximately the same voltage level. R_F is

the feedback resistor, which can be a passive resistor or a FET with the voltage at the gate controlling the feedback. The final section is another unity gain source follower stage with an active load. It acts as a buffered output for either improved current drive or impedance matching to the next stage.

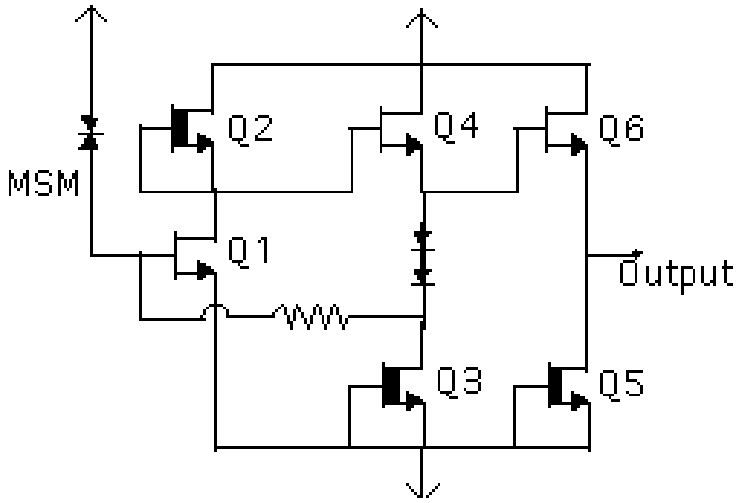


Figure 2.17 Transimpedance Amplifier Topology

The gain of the amplifier is determined by the equation

$$\frac{V_{out}}{I_P} = \frac{-R_F}{1 + \frac{jwR_FC_T}{1+A}}. \qquad (2.3)$$

R_F is the feedback resistance of the amplifier. A is the open loop gain of the inverting stage, and C_T is the total capacitance located at the input of the amplifier. The total capacitance at the input consists of the capacitance of the detector, C_d, the capacitances present at the gate of the input FET, $C_{gd} + C_{gs}$, the parasitic capacitance of the feedback

amplified by the gain of the amplifier, $(1+A)C_F$, and any stray wiring capacitance resulting from bonding pads and other parasitics, C_p

$$C_T = C_d + (C_{gd} + C_{gs}) + (1 + A)C_F + C_p. \quad (2.4)$$

Typically, the feedback capacitance is small and neglected for simplicity. However, in active feedback where a FET is used as a voltage-controlled resistance, the capacitance is higher than that of passive resistors. The 3dB bandwidth can be extracted as

$$f_{3dB} = \frac{1 + A}{2\pi R_F C_T}. \quad (2.5)$$

The stability of the first stage of the optical preamplifer is dependent on the same values that determine the frequency response. The loop gain and the feedback resistor help determine the stability of the first stage amplifier. The smaller the feedback resistor, the higher the gain but the lower the stability. Phase margin is significantly reduced when less feedback is present in the circuit.

The feedback helps determine stability but it isn't the only influence. From the preceding discussion, it is evident that the gain of the amplifier is provided by a single inverting stage. Although it is desirable to increase the gain of the amplifier by cascading gain stages, each additional stage will add a phase shift to the overall response, thereby cutting into the phase margin. This may cause the amplifier to oscillate, and therefore the gain stages are usually limited to one or two [2].

The input capacitance of the detector and input FET determines the equivalent input noise of the amplifier. Assuming that the thermal noise of the input FET is the most significant contributor of noise, it can be shown that the input-referred noise is minimized when the input capacitance of the FET matches the detector capacitance [24].

Although low noise operation was not the primary design consideration of this design, we examine the contributors to front-end noise as a starting point of the circuit design. The optical preamplifier, consisting of the detector and transimpedance amplifier, is the limiting factor in determining the sensitivity of the overall receiver. There are four factors that influence the overall noise of the preamplifier. The first is the thermal noise current of the feedback resistor in the transimpedance amplifier. The photodiode contributes it's own noise current and in this application it is from the dark current of the MSM. The input transistor has a noise current from gate leakage. And finally the noise of the preamplifier is determined by the overall noise of the amplifier, which is determined by the topology chosen.

The Gunning Transceiver Logic (GTL) output buffer provides for low on-chip power dissipation with the capability to drive large loads.

Gunning Transceiver Logics

Gunning Transceiver Logic (GTL) is an interface developed to meet the needs of high-speed digital systems. It is a low-swing system designed to increase the speed of data buses, reduce noise, and minimize power consumption. Table 2.2 compares the high and low states of various digital families. GTL buffers are designed for relatively low output capacitance (5pF max) in comparison with a TTL output buffer (up to 15pF).

Higher output capacitance contributes to the overall capacitance of the transmission line, reducing the characteristic impedance. Low characteristic impedances require more current from the driver circuits, making it difficult to realize high-speed signals.

Table 2.2 Comparison of Voltage Logic Levels

Logic	Vout High Minimum	Vout Low Maximum
CMOS	3.8 V	0.44 V
TTL	2.4 V	0.55 V
BTL	2.1 V	1 V
GTL	1.2 V	0.4 V

Many factors contribute to the power consumption of a device. Compared with other low voltage swing logic, GTL has lower power consumption [25]. Table 2.3 shows a power comparison of BTL and GTL driving 160 active I/Os.

Table 2.3 Comparison of Power Usage of BTL and GTL

Technology	Power (Watts)	Termination
BTL	11	50 Ohm to 2V
GTL	1.5	50 Ohm to 1.2V

A schematic diagram of a single channel of the photoreceiver circuit is shown in Figure 2.18. The input transimpedance amplifier is composed of Q1 and Q2 and is based on a design from [26]. The resistor R2 sets the transimpedance of the input stage and was selected to provide a basic light threshold level of approximately 100 μW. R2 functions as feed back. Additional adjustments can be made through R1. An input offset current can be injected to adjust the receiver threshold level. Following the transimpedance amplifier is a simple decision circuit. The decision circuit controls the output buffer,

which is large enough to be able to drive the following circuitry. The output buffer consists of a two buffer stages. The first stage is a driver for the large open drain GTL output buffer. Since the output transistor is either entirely "on" or "off" and the GTLs voltage swing is approximately 0.8V, very little power dissipation occurs on the die due to the output buffers.

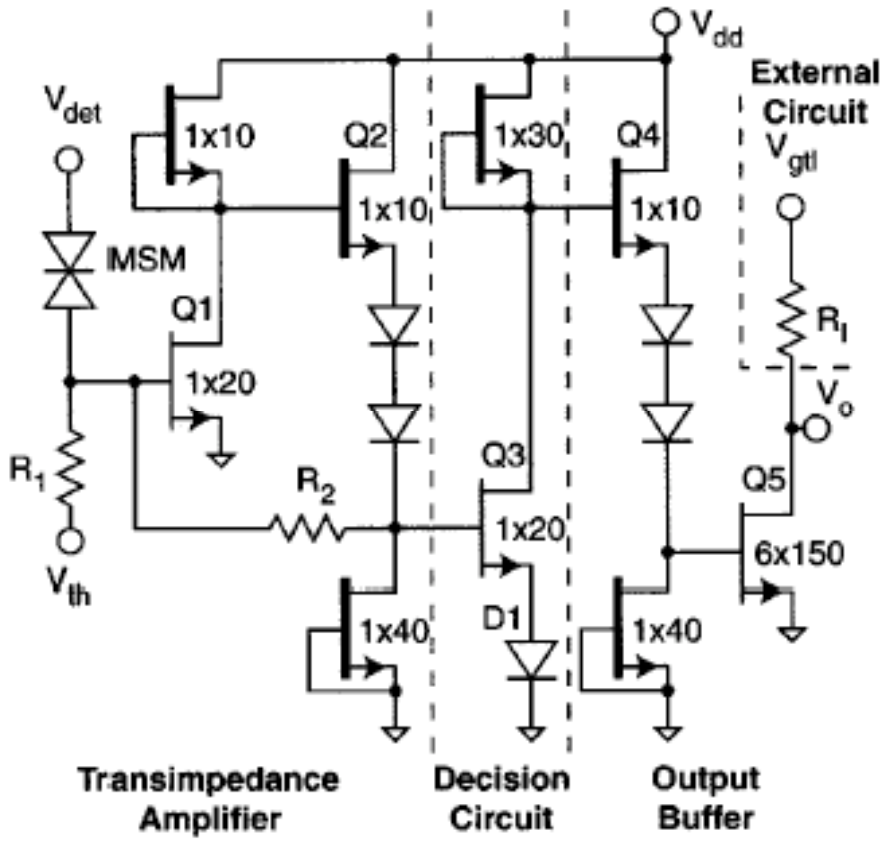


Figure 2.18 Photoreceiver Schematic

A microphotograph of the 8x8 photoreceiver array is shown in Figure 2.19. The total die size is 3800 um x 3800 um with a total power dissipation of less than 2W using a 3V supply. The center of the die contains the array of photodetectors. The

transimpedance amplifiers and buffer circuits are spaced along the die periphery. The skew of channel is minimized but not eliminated by judicious choice of layout for connects between amplifiers and photodetectors.

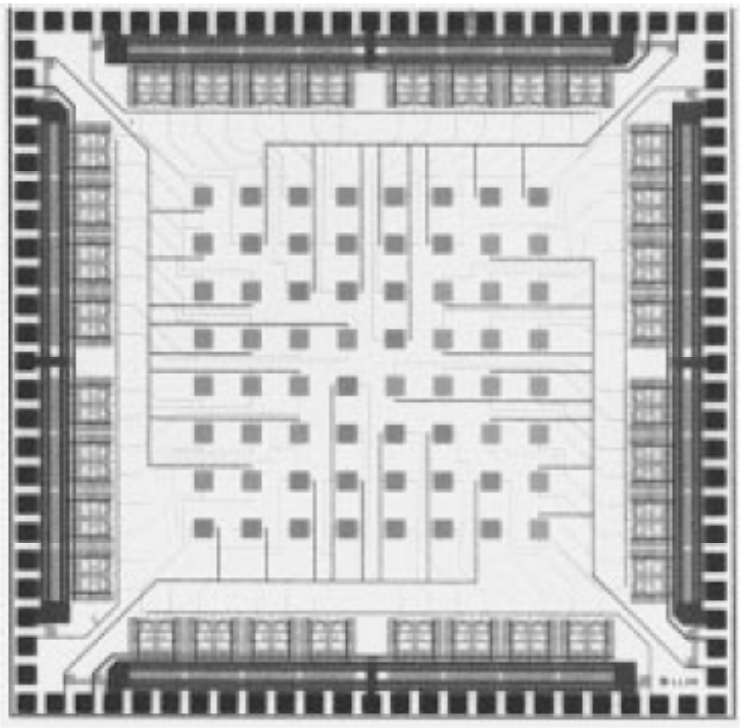


Figure 2.19 Photograph of 8x8 Photoreceiver Array

Figure 2.20 shows a received signal of one of the channels of the array. The data was transmitted at 1 Gb/s.

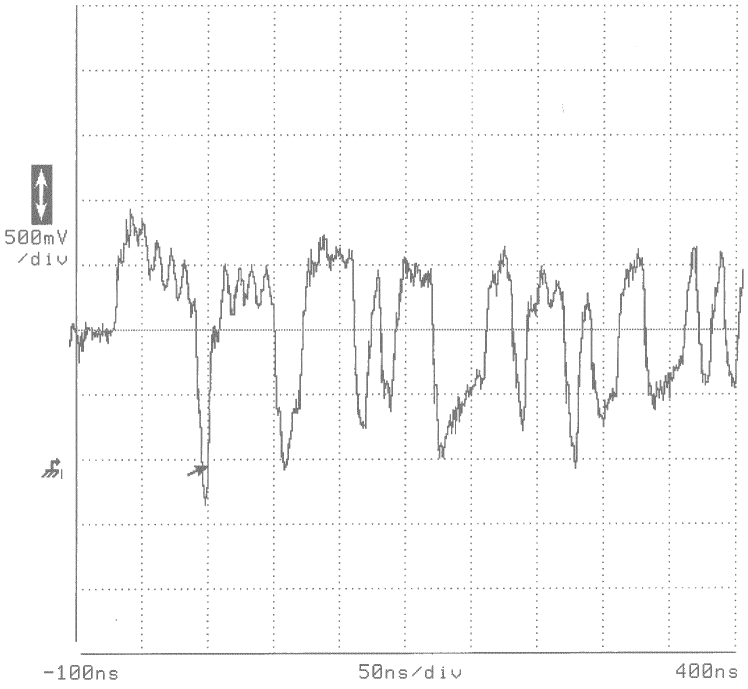


Figure 2.20 1 Gb/s Signal

CHAPTER 3

LONG HAUL TWA RECEIVER FRONTEND

Background

The rapidly increasing demand for data is driving the need for high data rate networks. In the near future, current systems will not be able to provide the level of performance required and in response, new standards have been defined for 40 GB/s and higher data rates. High-speed photoreceiver front-ends for long wavelength systems are expected to play a major role in these telecommunication systems. To handle these data rates, high-frequency designs with broad bandwidths are needed to accommodate the digital signals. Several circuit topologies have been successfully used for front-end amplifiers with bandwidths in the tens of GHz. The transimpedance topology is a familiar and popular single-stage design used in optoelectronic receivers. Another design used more recently to implement the wider bandwidth designs is the distributed amplifier.

The photodetector is a critical component in optical communication systems. There are many choices of photodetectors available to the designer. The choices can be divided into edge illuminated waveguide photodetectors and vertically illuminated photodetectors. Optical signals are fed parallel to the substrate through the sides for edge-illuminated photodetectors. Edge illuminated waveguide photodetectors include travellingwave photodetectors. Launching a signal from a fiber into a waveguide structure can be difficult to do without suffering significant coupling losses. In contrast,

vertically illuminated photodetectors have the light incident perpendicular to the surface and generally more applicable for low loss fiber optical receivers.

The MSM detector from the previous chapter is an example of one type of vertically illuminated photodetectors. They are well suited for high performance optical communication links because of their low capacitance per unit area, which enables high speed operation. Unlike P-I-N vertically illuminated photodetectors whose relatively high capacitance per unit area necessitates smaller detectors for high speed operation, MSMs can also be built with relatively large detection areas without severely impacting the speed of operation. However because of the structure of MSM photodetectors, there can be a problem with finger electrodes shadowing the substrate and reducing the amount of light that is collected. To increase responsivity, one technique is to use inverted thin-film photodetectors [27-29].

Flip chip bonding is one hybrid technology that has been used for OEIC applications [30-31]. Another process is thin film device bonding where only the epilayers of the bonded device are used and the bonding metallization is on the order of the contact thickness, rather than the thicker solder bumps. The thin film process enables the ability to utilize novel structures to improve overall circuit performance, such as in this case, removal of the InP substrate for higher responsivity detectors. An inverted MSM structure (I-MSM) has shown to provide alignment tolerance for detector to fiber connections relaxing the stringency on the packaging requirements

Thin Film MSM Photodetector

One method for integrating semiconductor devices with dissimilar host substrates is thin film device integration. Semiconductor devices can be separated from the growth substrate and bonded to a new host substrate using standard microelectronic process.

Inverted thin-film MSM photodetectors has the growth substrate removed so that the MSM can be inverted for backside illumination and attached to a new substrate. Inverting the MSM puts the contact fingers on the bottom of the device and out of the way of the incident light. The MSM is then bonded directly to receiver circuits. The benefits of this technique are that responsivity is improved and that near monolithic performance can be achieved without being limited to a single material system. The photodetector material can thereby optimized for performance without adversely affecting circuit performance. The receiver circuitry can be designed on the most cost effective material system for the performance required.

Thin film devices are typically semiconductor components where the substrate is removed. The substrate is necessary for growth and physical stability of many devices but seldom contributes to the functionality. The active layers can be separated from substrate with minimal detriment. The devices in the active layer are typically several microns thick and can be bonded or attached to substrates of arbitrary composition to fabricate multimaterial OEICs with near monolithic performance.

The technique to separate the thin film epitaxial material from the substrate is a chemical process. Either a sacrificial layer is selectively etched to separate the active layers or the substrate is etched away with a stop etch layer to protect the active devices. The different layers, stop etch layer or sacrificial layer, will have a significantly different

etch rate from neighboring layers thereby enabling selectivity when using different etch solutions.

Figure 3.1 diagrams the process for substrate removal. The layer structure consists of the growth substrate, a stop etch layer that is as closely lattice matched to the substrate as possible, and the epitaxial active layers of the device. The active devices are fully fabricated and completed with metal contacts. Apiezon W black wax is used to cover and protect the devices and aids in handling of the thin film. A chemical etch is used to remove the substrate. This first chemical etch rapidly removes the substrate but is much less reactive with the stop etch layer thereby controlling the etch process. The stop etch is then removed with a second selective chemical etch that rapidly consumes the stop etch layer but has minimal reaction with the active layers. The devices are subsequently bonded to a mylar transfer diaphragm via contact or van der Waals bonding. At this point, the top surface and metallization are facing away from the diaphragm. The devices can then be transferred to a new host substrate and bonded with circuitry.

The use of a transparent Mylar diaphragm as an intermediate transfer medium is an improvement over the basic process of thin film bonding. The transfer diaphragm technique utilizes the thin-film devices in an effective manner since many host substrates can be serviced with one thing film array of devices. Since the the devices are inverted and an array of devices can be aligned and selectively bonded, both sides of the thin-film devices can be processed on either the original growth substrate or the new host substrate. This is beneficial in bonding since the side of the device metallized before separation is now bonded to the new host substrate. The facilitates a stable electrical and mechanical bond when the metal/metal contact between device and circuitry is annealed.

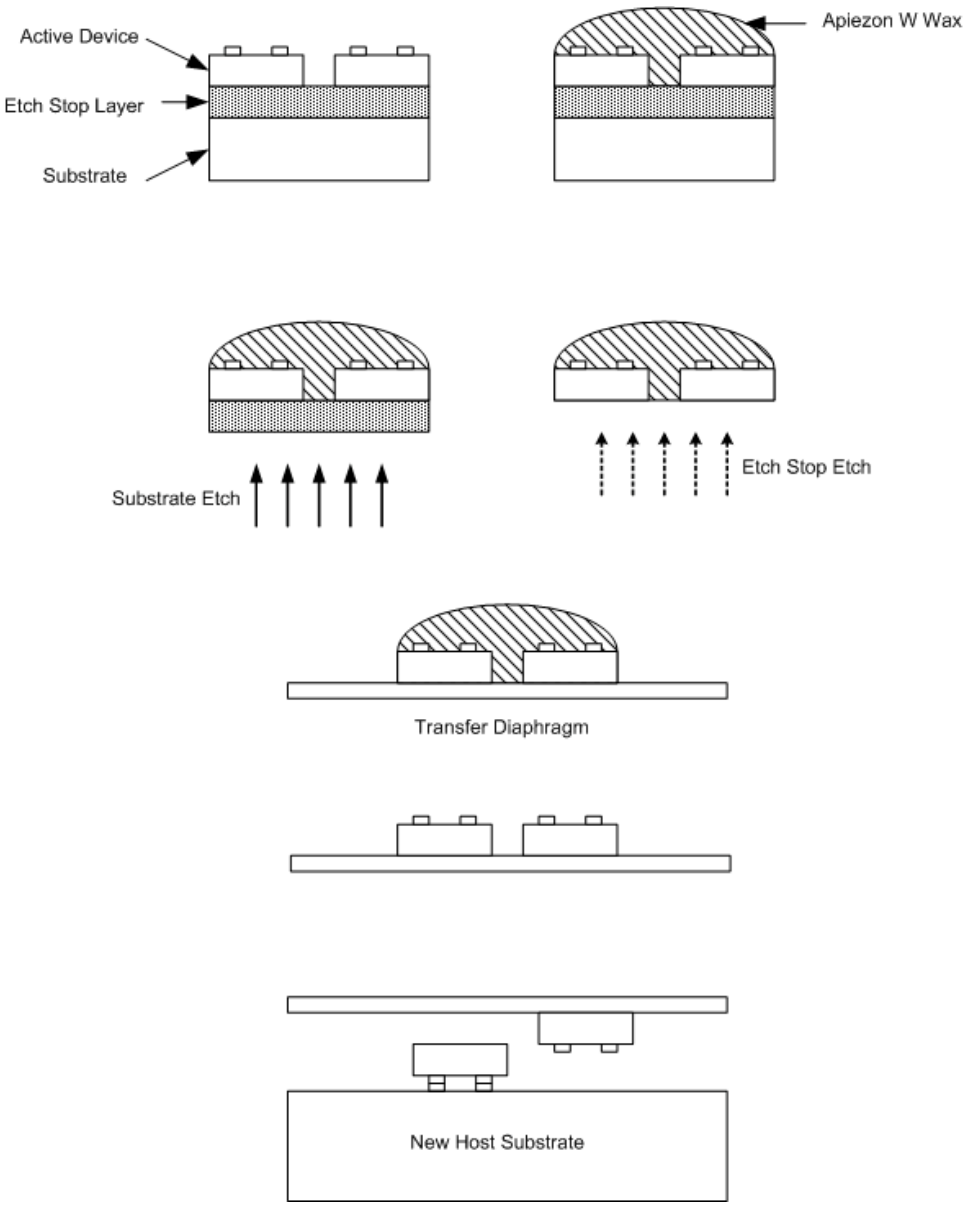


Figure 3.1 Thin-Film Integration Process

The MSM for this receiver consisted of a design optimized for I-MSM high responsivitity and high speed operation. The MSM is fabricated on a double heterostructure lattice with a sacrificial etch layer. The layer structure consists of an InP substrate, InGaAs 100nm etch stop layer, InAlAs 40nm active layer, InGaAs 1000nm active layer, and InAlAs 40nm active layer. The MSM diameter is 50 μm. The Ti-Au contact fingers are 1 μm wide with 1 μm spacing. The InP growth substrate was selectively etched with HCl. The devices remain protected by the covering of Apiezon W wax and the InGaAs stop etch layer. The etch stop layer is subsequently removed using a citric:H2O2(1:1) selective etch. The MSMs are bonded to a mylar transfer diaphragm and the wax is removed. The devices are then aligned and bonded to the host substrate and the samples are annealed to form a high quality electrical and mechanical bond [27].

When the performance of the I-MSM is compared with a conventional MSM, it is shown that responsivity is maximized without trading off speed of operation. With geometries that allowed about 50% finger coverage, the I-MSM showed approximately 3 times improvement in responsivity. Previous results on I-MSM performance on two MSM photodetectors with exactly the same device geometry show that the I-MSM achieves a 0.7 A/W responsivity compared to a 0.23 A/W responsivity for a conventional MSM structure [27]. Not only does the inverted structure benefit from absence of finger shadowing but light is also reflected back into the photodetector material. The dark currents for both devices are less than 15nA and so no appreciable noise is incurred when using a thin film device. The measured transient response of the photodetectors shows about a 30% slower reaction time for the I-MSM. The conventional MSM have a rise

and fall time of 27 ps and 61 ps, respectively. The I-MSM demonstrate a rise and fall time of 34 ps and 85ps, respectively [37]. While the inverted structure is slightly slower than the conventional photodetector for the same finger spacing, this can be overcome in the I-MSM by reducing the finger spacing to improve speed without affecting responsivity (which can't be done with a regular MSM).

For the integrated photoreceiver, the first step in the design was to characterize the electrical operation of the MSM. When operating well below the cutoff frequency of the detector, the photo-detector can effectively be modeled as a simple current source. However in these applications and for our MSM, frequency response has a significant effect upon the design. The MSM was modeled to generate a small signal model for circuit simulations. An empirical model was generated with experimental techniques. Coplanar waveguide (CPW) structures were fabricated on a silicon wafer and the detector was bonded onto this structure. This permitted on-wafer probes to measure the S-parameters of the CPW structures with the photodiode and the CPW structures alone. Figure 3.2 shows the S-parameter measurements of the CPW structure and the photodiode.

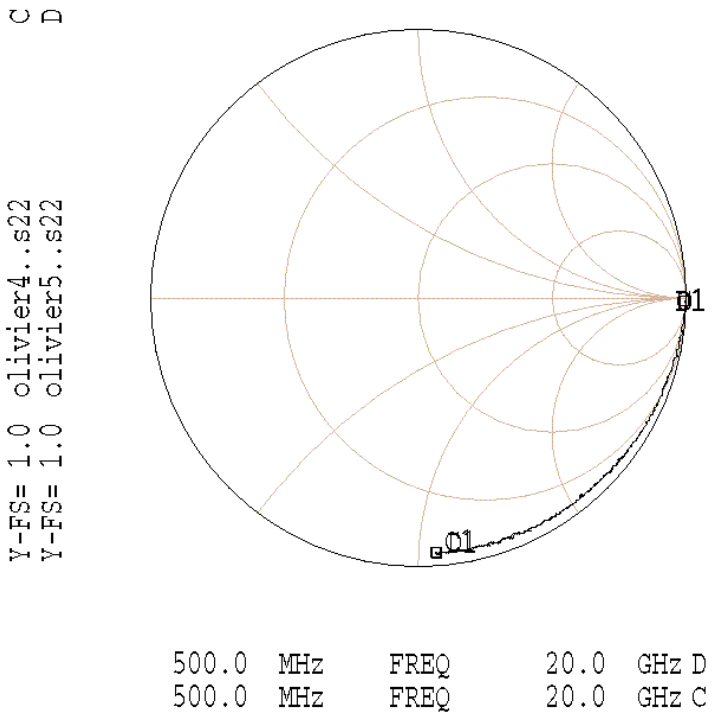


Figure 3.2 Measured S-parameters of Photodiode

The detectors were biased and a single port S-parameter measurement was made with a network analyzer. From the collected S-parameters, the capacitance was extracted by converting the S-parameters into impedance and calculating the capacitance from the imaginary portion. The measured capacitance of the CPW structure was subtracted from the measured capacitance of the combined CPW structure and photodiode. The extracted MSM capacitances for two measurements are shown in Figure 3.3. The measurements confirm an extracted capacitance of approximately 10 fF for the MSM.

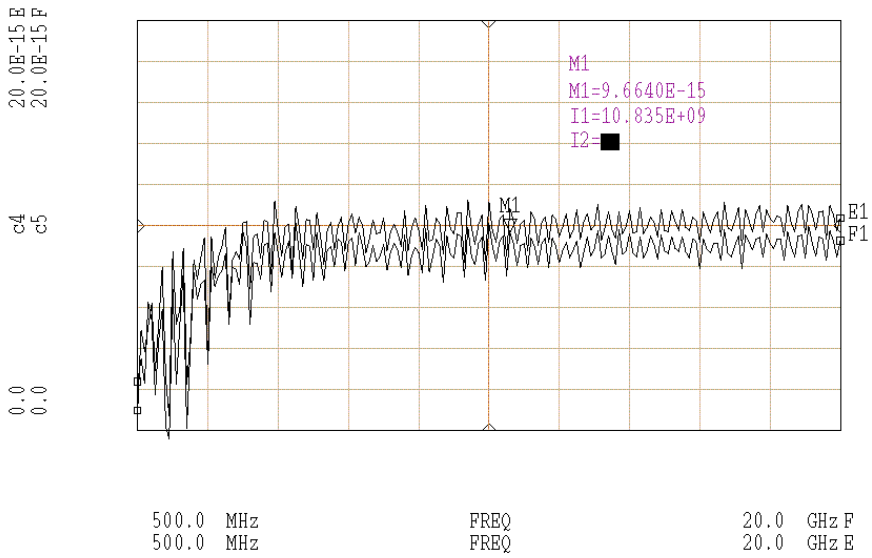


Figure 3.3 Extracted Capacitance of MSM

A simple circuit model was generated from this measured data. For the subsequent circuit simulations, the photodiode was assumed to be fairly frequency independent and was modeled as a current source with a shunt capacitance as shown in Figure 3.4.

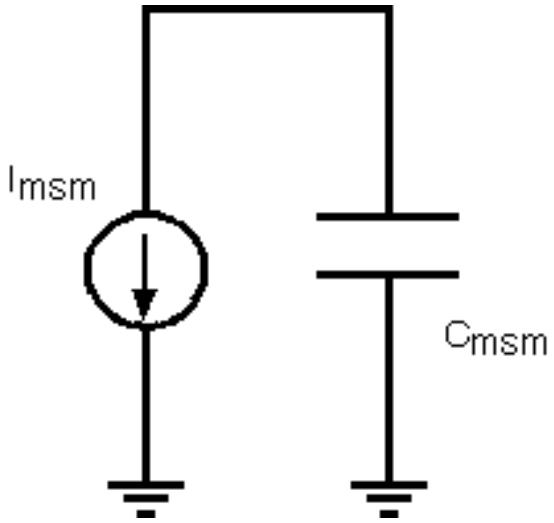


Figure 3.4 Simplified MSM Circuit Model

Transimpedance Amplifier

Once the detector is chosen, the rest of the circuit is designed around those parameters. The first topology chosen was the basic transimpedance amplifier as shown in Figure 3.5. The needs of the circuit demanded widest possible bandwidth, adequate sensitivity, and high gain but did not require a wide dynamic range. Amongst the topologies available the simplest choice was the basic transimpedance amplifier.

The size of the input FET determines the current running through the input FET. An active current load is designed by consulting simulated DC curves to determine the width of the transistor to maintain the proper current through the input transistor. The next stage is the source follower stage, designed with nominally the same sized transistors as the first stage. Level shifting diodes are added between the active load and the source follower FET to maintain proper DC biases between the two stages. During the initial stage of the design, the voltage drop across the diodes was nominally taken as 0.7 V. The final stage is an output match stage and is designed for a 50 Ω impedance.

The entire circuit was simulated with Agilent's microwave circuit simulation tools. Simulations were used to optimize the operation of the circuit. The DC operation was refined such that no transistors were biased into shutoff or beyond operating tolerances. The final output stage was optimized for 50 Ω termination.

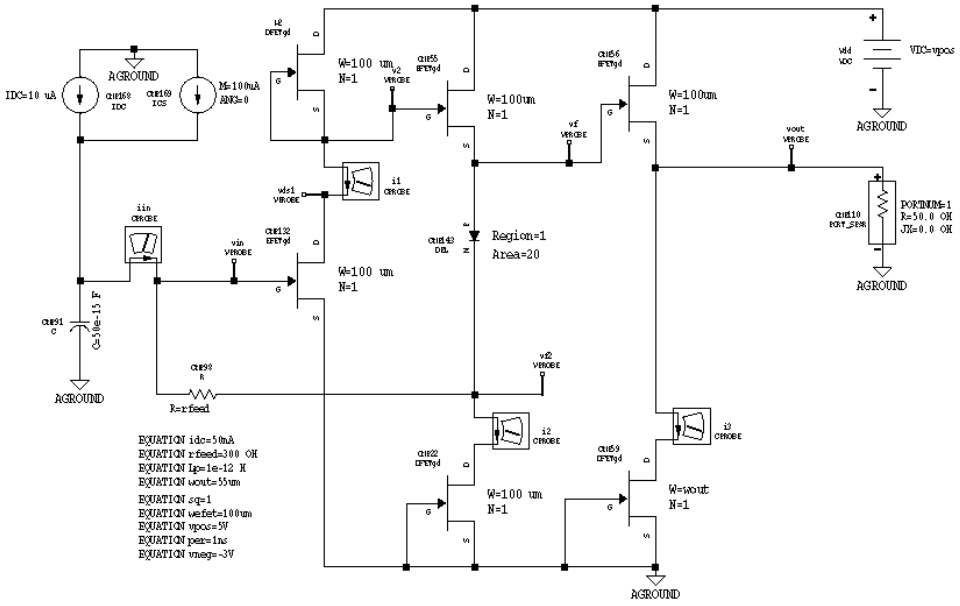


Figure 3.5 Transimpedance Amplifier Circuit

Figure 3.6 is a photograph of the GaAs transimpedance amplifier circuit after integration with the thin-film I-MSM detector. An Agilent 8703A lightwave analyzer was used to measure the OEIC's small signal bandwidth. The lightwave analyzer adds optical capabilities to the microwave network analyzer. It is capable of measuring S-parameters as well as incident, reflected, and transmitted optical power. The optical signal is fed by a single mode fiber from the lightwave analyzer's optical laser source to the detector and on-wafer coplanar waveguide (CPW) probes were used to extract the electrical signal. The lightwave analyzer measured the ratio of the incident optical power

to the transmitted electrical power or the equivalent of the optical to electrical S21. Using a 1.55 μm laser source, measurements of the frequency response, shown in Figure 3.7, revealed a -3dB bandwidth of 1.5 GHz.

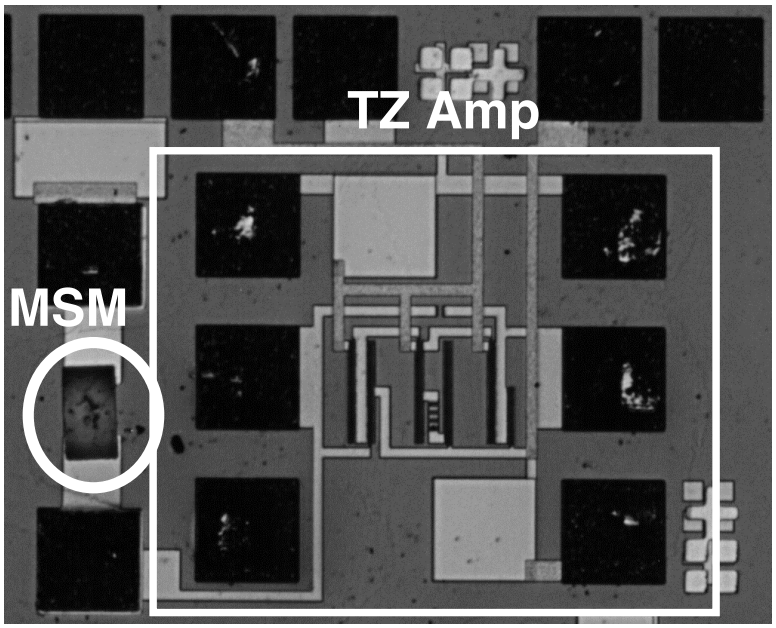


Figure 3.6 Integrated Transimpedance Receiver

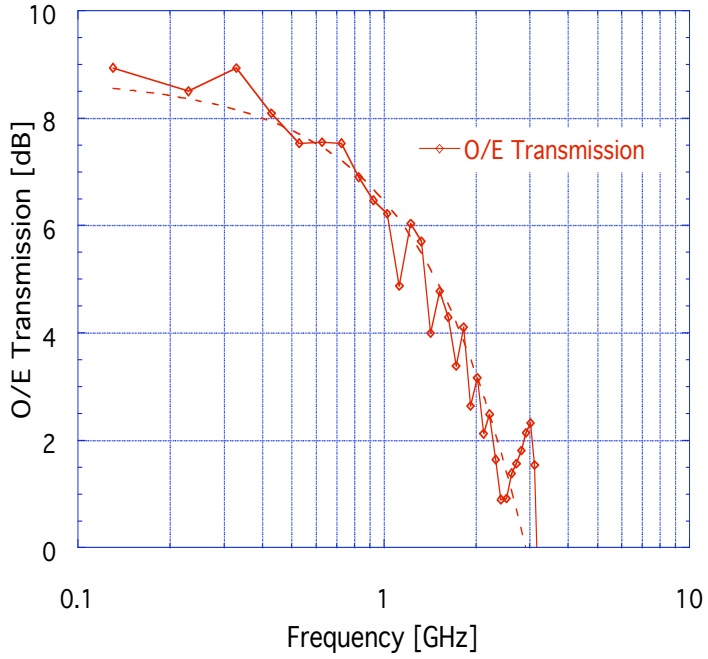


Figure 3.7 Measured Optical to Electrical Response of Integrated Receiver

Although transmission gain and bandwidth provide an indication of how well a receiver will perform, a more accurate characterization can be obtained with a bit error rate tester (BERT) and an oscilloscope. The BERT generates an optical pseudo-random digital signal. This signal is fed into the amplifier, and the electrical output is read by the oscilloscope. A clock signal from the BERT allows the time dependent waveform to be overlaid upon each other synchronized upon each clock cycle. As the waveforms are overlaid upon one another, any imperfections in the signal will close the gap between the high and low signals or the "eye" of the waveform. Figure 3.8 shows an open eye diagram of the receiver with a 1 Gbps pseudo-random data stream (up to 2^{31}-1). As the data-rate of the optical signal is increased to 2.4 Gbps, the eye begins to close as shown

in Figure 3.9. Above 2.4 Gbps yields a closed eye diagram which indicates the receiver is too slow for such data-rates.

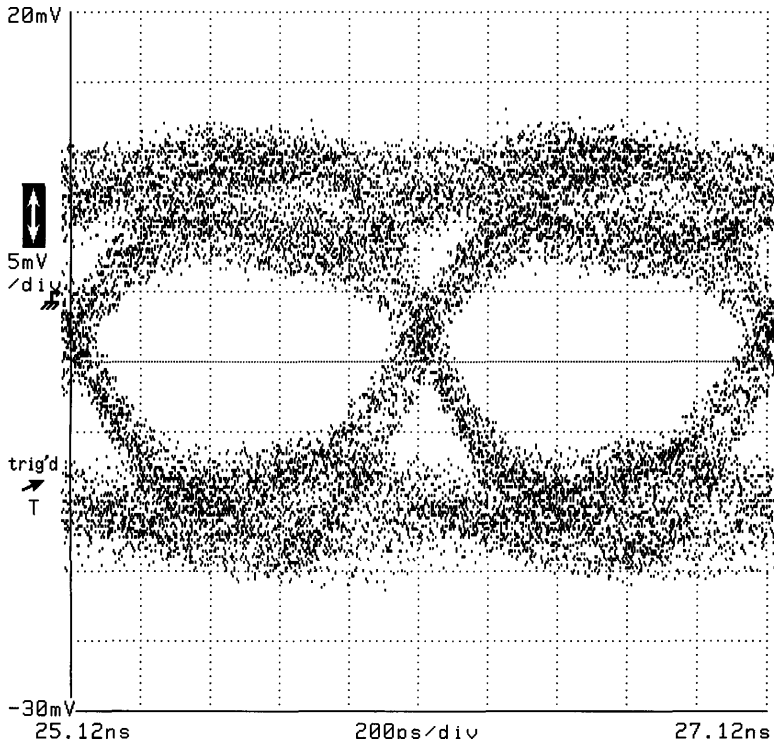


Figure 3.8 Measured Eye Diagram at 1 Gbps

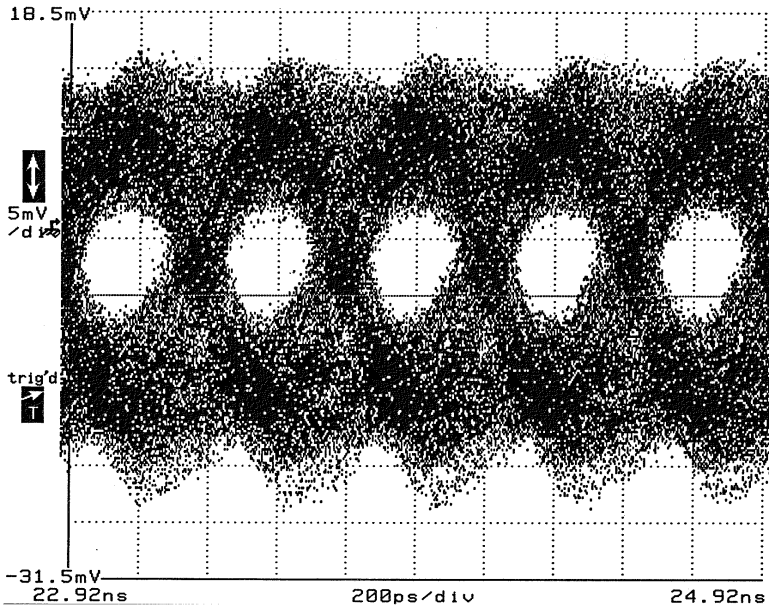


Figure 3.9 Measured Eye Diagram at 2.4 Gbps

Travelling Wave Amplifier Background

The simulated performance did not approach the eventual design goal of 10 Gbps. To begin efforts toward higher data rate front-ends, design of a TWA photoreceiver was initiated. Using the guidelines presented in the theory section, a first pass design was generated. However, because the guidelines include numerous assumptions that simplify FET characteristics, simulation was used to further optimize the circuit design. The transmission lines that connect the different stages are optimized to obtain the best gain flatness and bandwidth. The design equations only provide a starting point for the design of the TWA.

The principle of distributed or travellingwave amplification using discrete transistors is a technique whereby the gain bandwidth product of an amplifier may be increased. The amplifier can be designed to give a flat, low pass response up to very high frequencies. When FETs are combined in parallel to increase the gain, the gain is

increased but the capacitances add, thereby resulting in no net increase in the gain-bandwidth product. In the distributed amplifier, the input and output transistor capacitances are not added when stages are cascaded together. With this approach, the input and output capacitance of the transistors are combined with inductance from transmission lines or formed by lumped inductors to create artificial transmission lines. The signal is amplified by the transistors and combined coherently along the artificial transmission lines.

Distributed amplifiers using discrete transistors have demonstrated at various frequencies and with various transistor technologies [32-35]. The topology of the distributed amplifier is well suited for integrated circuit implementation because the inductance required to form the artificial transmission line is easily realized on chip in the form of transmission lines or passive inductors and the repeatability of active and passive devices minimize the need to tune to correct for variations in the components. The design of the TWA involves choosing the device, the number of devices, and the impedances and cutoff frequency of the lines.

A simple schematic representation of the distributed amplifier is shown in Figure 3.10. Lossy artificial transmission lines are formed by the lumped inductors and the gate and drain capacitances. The lumped element model of a transmission line is shown in Figure 3.11. Figure 3.12 illustrates the distributed amplifier topology and how the transmission lines and the parasitic capacitances of the FET approximate a transmission line.

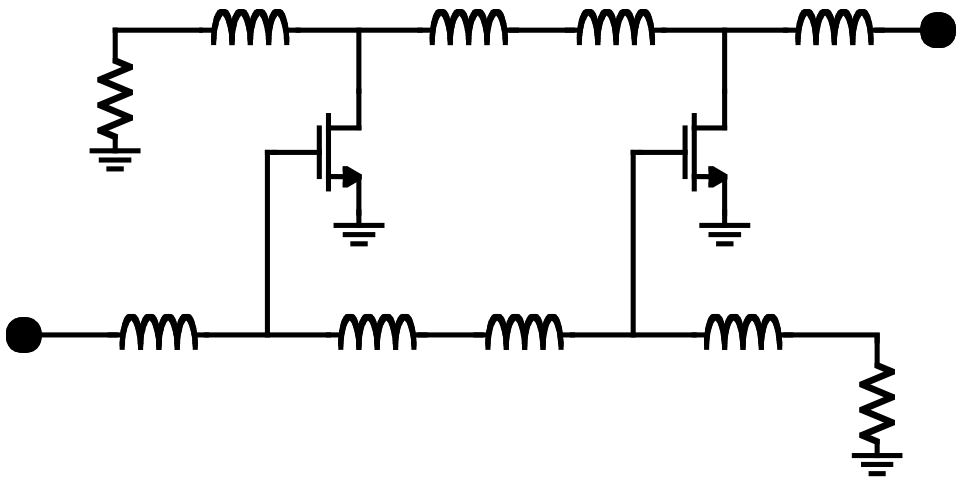


Figure 3.10 Travelling Wave Amplifier Topology

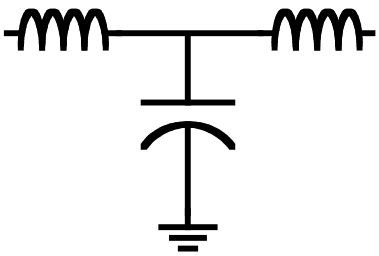


Figure 3.12 Lumped Element Transmission Line Model

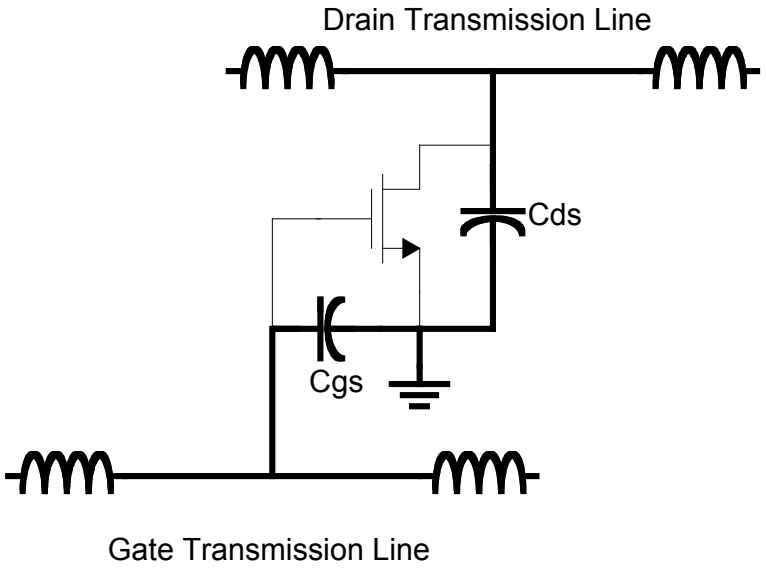


Figure 3.13 Artificial Transmission Lines Formed by TWA

The resulting transmission lines are referred to as the gate and drain lines respectively. These two transmission lines are then connected via the gain of the transistors. The input signal is sent down the gate line. Along the way, the signal drives the transistors and the signal is amplified to the drain line. The signal then travels down the drain line to the output. As the transistors amplify the signal, each transistor amplifies at different phases because of the delay resulting from the transmission line. If the phase velocity of the signal at the drain line matches that of the gate line, then the signal will add in the forward direction of the drain line [36].

The characteristic impedances of the gate and drain lines can be approximated with the equations

$$Z_g \approx \left[\frac{L_g}{(C_g + C_{gs}/l_g)}\right]^{0.5} \tag{3.1}$$

and

$$Z_d \approx \left[\frac{L_d}{(C_d + C_{ds}/l_d)} \right]^{0.5} . \qquad (3.2)$$

The inductance and capacitance per unit length of the transmission lines at the gate and drain are represented by L_g, L_d, C_g, and C_d. The lengths of the gate and drain transmission lines are l_g and l_d respectively. Cgs and C_{ds} are the gate and drain parasitic capacitances in the simplified MESFET model shown in Figure 3.13.

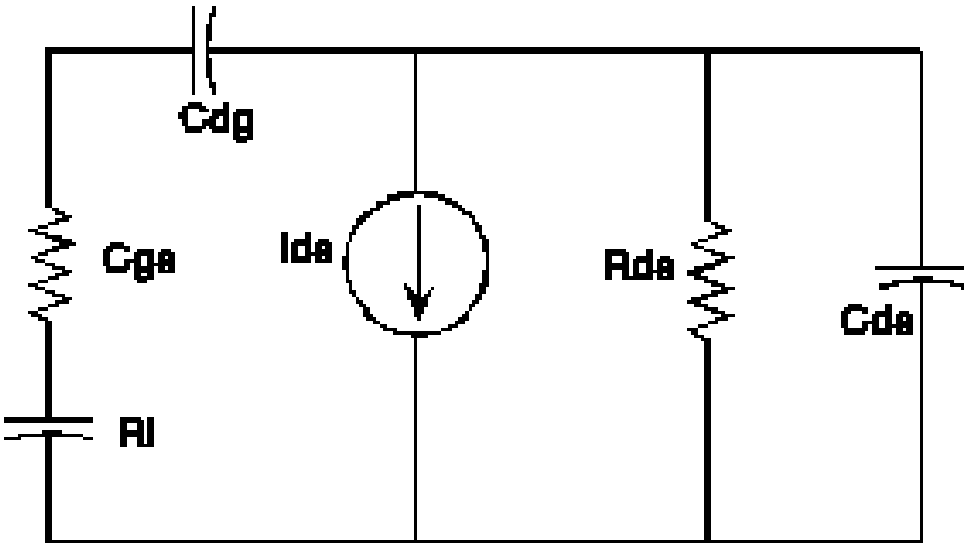


Figure 3.13 Simplified MESFET Model

The input signal is then terminated at the end of the gate line with a matching termination to prevent reflection. When the forward phase velocities of the gate and

drain lines are identical, the signals on the drain line add together in the forward direction. The signals travellingin the reverse direction are out of phase and are absorbed by the drain line termination.

To analyze the topology, the gate and drain transmission lines are considered constant-k lines. The assumptions made are that the parasitic resistances in the FET are the primary loss mechanisms and that the lines are terminated with their image impedances. The voltage across C_{gs} of the kth transistor can be derived from the current delivered to the load [37]

$$V_{ck} = \frac{V_i e^{-(2k-1)\theta_g/2 - j\tan^{-1}(\omega/\omega_g)}}{\left[1+\left(\frac{\omega}{\omega_g}\right)\right]^{1/2}\left[1-\left(\frac{\omega}{\omega_c}\right)\right]} \tag{3.3}$$

V_i is the input voltage and θ_g is the propagation function of the gate line. The propagation function tracks the attenuation and phase shift on the gate line. When the phase velocities of both the gate and drain lines are designed to be equal, the power gain of the amplifier can be determined [37] to be

$$G = \frac{g_m{}^2 Z_d Z_g \sinh^2\left[\frac{n}{2}\left(A_d - A_g\right)\right]\exp(-n(A_d + A_g))}{4\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]\sinh^2\left[\frac{1}{2}(A_d - A_g)\right]} \tag{3.4}$$

where A_g and A_d are the attenuation of the gate and drain lines, respectively, and ω_g and ω_d are the cut-off frequencies of the gate and drain lines, respectively, in radians. From the power gain of the amplifier, the voltage gain of a single amplifier stage can be determined to be the Equation 3.5.

$$A = \frac{g_m\left(Z_d Z_g\right)^{1/2} \sinh\left[\frac{n}{2}\left(A_d - A_g\right)\right] \exp(-n(A_d + A_g)/2)}{2\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]^{1/2}\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]^{1/2} \sinh\left[\frac{1}{2}(A_d - A_g)\right]} \qquad (3.5)$$

The result of this equation highlights the fact that the gain of the TWA cannot be increased indefinitely by adding more stages. The loss in the gate line eventually attenuates the signal so much that the gain of the transistor is insufficient to boost the signal to a usable level on the drain line. Therefore subsequent stages of transistors do not contribute any more signal power to the output and in fact only contribute additional loss to the drain line.

From Equation 3.5, it has been shown that the optimum number of stages that will maximize the voltage gain can be determined from the equation [38]

$$N_{opt} = \frac{\ln(A_d / A_g)}{A_d - A_g} \qquad (3.6).$$

From the previous derivations, it becomes evident that attention to the attenuation of the drain and gate lines is necessary to shape the response of the amplifier. The phase

of the lines must be designed such that the signal adds at the output of the drain line. The attenuation of the lines determines the optimum number of stages for maximum gain. The frequency response of the amplifier is derived in part from the frequency response of the lines.

Because frequency response of a transmission line is within the control of the designer, the frequency response of the amplifier can be controlled by engineering the response of the gate and drain transmission lines, as well as controlling the number of cascaded stages. Proper design of the transmission lines strives to result in a flat amplifier response nearly up to the cut-off frequency of the lines. The degree of flatness is defined as the -1dB bandwidth normalized to the cut-off frequency, also called the fractional bandwidth. By mapping lines of constant fractional bandwidth, transmission line characteristics can be chosen that will result in a desired flatness response of the amplifier.

Cascode TWA

One of the limiting factors of very broadband TWAs is the loss in the drain and gate lines. A technique used to extend the broad bandwidth of the TWA is the use of a cascode pair of transistors [39]. Broadband losses in the drain line are compensated by the common-gate transistor of the cascode transistor. Figure 3.14 shows the cascode pair topology. The cascode pair works by adding a negative resistance to overcome losses in the circuit.

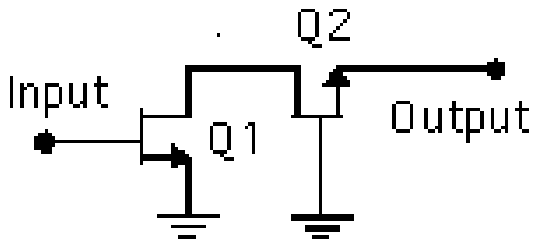


Figure 3.14 Cascode Pair

It has been shown through analytical studies of the conventional TWA that the line attenuation parameters control the gain and the bandwidth. Active impedances inserted along the loaded transmission lines can affect the attenuation characteristics. The addition of frequency dependent reactances and negative resistances compensate for signal losses dominated by the positive transistor input resistances and drain resistances. Reduction of the attenuation connecting the stages allows for more sections to be cascaded, resulting in an increase of maximum output power. The broad-band loss compensation of the gate and drain lines permits an extension of the maximum bandwidth.

The FET in the common gate configuration generates the negative resistance that is used to cancel transmission line loss. It can be shown that the impedance at the drain of the common-gate FET has a negative term [39].

$$Z_{nr} = \frac{R_{ds}}{1 + j\omega C_{ds} R_{ds}} + \frac{1}{j\omega C_{ds}} + R_i + Z_g + \frac{g_m R_{ds}}{j\omega C_{gs}\left[1 + j\omega C_{ds} R_{ds}\right]} \qquad (3.7).$$

The real portion of the last term is calculated to be

$$-\frac{g_m R_{ds} / \left(\omega_d C_{gs}\right)}{\left(1 + j\omega / \omega_d\right)\left(1 - j\omega / \omega_d\right)} \qquad (3.7).$$

When combined with the common source FET typically used in the TWA, several advantages become apparent. The common gate configuration provides additional gain and reverse isolation to the common source FET. The transmission line between the common source and common gate transistor adjusts the forward gain and the overall impedance of the cascode block.

The benefits of the cascode can be further improved by asserting more control over the expression of negative resistance. From equation 3.8, it can be seen that the negative resistance effective is determined by transistor parameters. To exert more control over the effect of negative resistance, transmission lines are added to the cascode topology. These transmission lines act as additional parasitic inductances and further refine the gain and impedance of the cascode cell.

For the TWA design, a readily available and mature GaAs MESFET process was used. The process chosen was TriQuint's GaAs ion implanted depletion mode MESFET process known as HA2. The FET gate lengths available are 0.5 μm and 1 μm. For the high speed operation we used the faster 0.5 μm gates. The cutoff frequency and maximum oscillation frequency of the process is 19 GHz and 60 GHz respectively. The interconnect metals can be stack to a 6.3 μm thickness to provide low loss interconnects. Metal insulator metal (MIM) capacitors, implant resistors, and NiCr resistors are readily available on this process. The process is useful for a wide variety of low noise and medium power applications.

Results

The TWA was designed in a commercial GaAs MESFET process. A cascaded topology was chosen designed. The MMIC was fabricated in TriQuint's HA2 process. This process is a GaAs implanted MESFET process utilizing depletion mode MESFETs with cutoff frequencies of approximately 20 GHz.

The circuit was designed using the guideline formulas presented above as a start with much refinement and optimization during simulations. The transmission lines were optimized to provide the matching phase in the gate and drain lines. Then the overall amplifier was optimized for bandwidth and gain. The final schematic is shown in Figure 3.15.

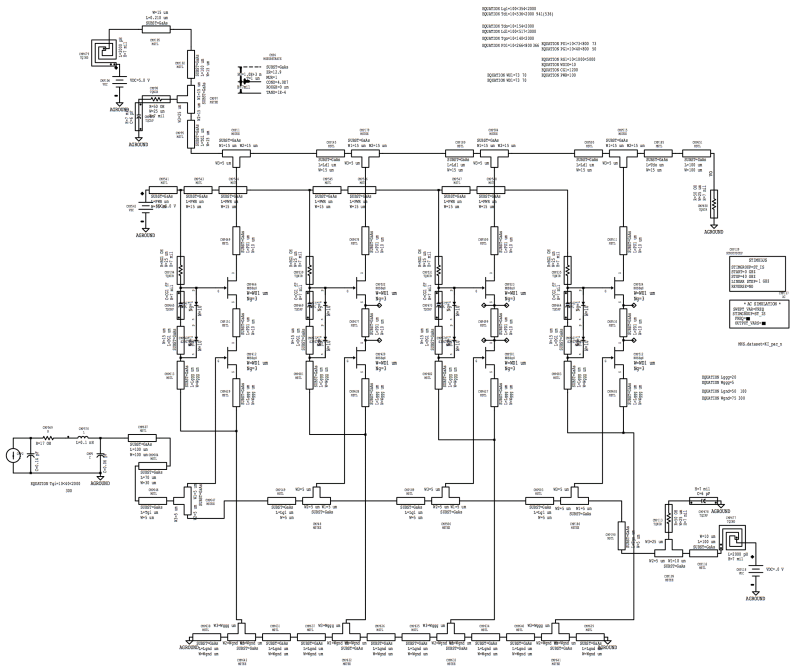


Figure 3.15 Schematic of TWA

The picture of the fabricated circuit is shown in Figure 3.16. To measure the receiver, the optical signal is fed by a single mode fiber to the detector and on-wafer coplanar waveguide (CPW) probes are used to extract the electrical signal. Generation of an eye determined with a HP8703A lightwave operation. A 1.55 μm single mode laser source directly modulated with a pattern generator sends an optical pseudorandom data stream (up to 2^{31}-1) to the receiver. As shown by Figure 3.17, the TWA has a measured bandwidth of 18 GHz and approximately 6 dB of gain with an HP8510C network analyzer and CPW probes. The return loss up to 18 GHz is below 10 dB at the input and output. The amplifier is driven by a single 3 V power supply and the power consumption of the amplifier is 45 mW. A 20Gb/s eye diagram is shown in Figure 3.18.

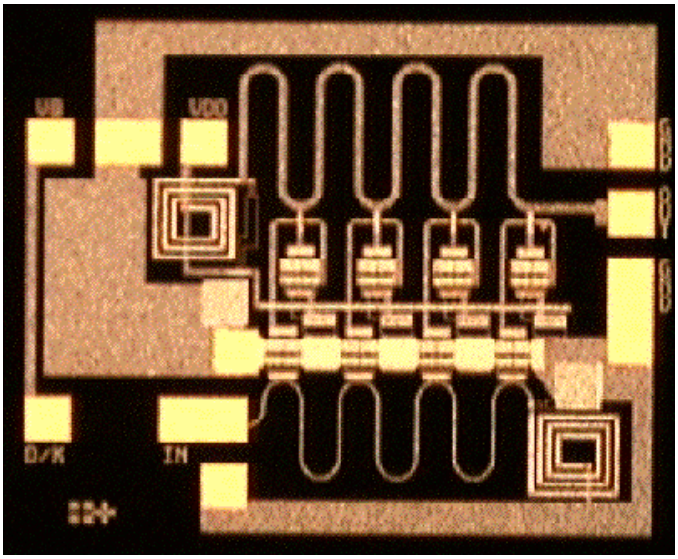


Figure 3.16 Photograph of TWA

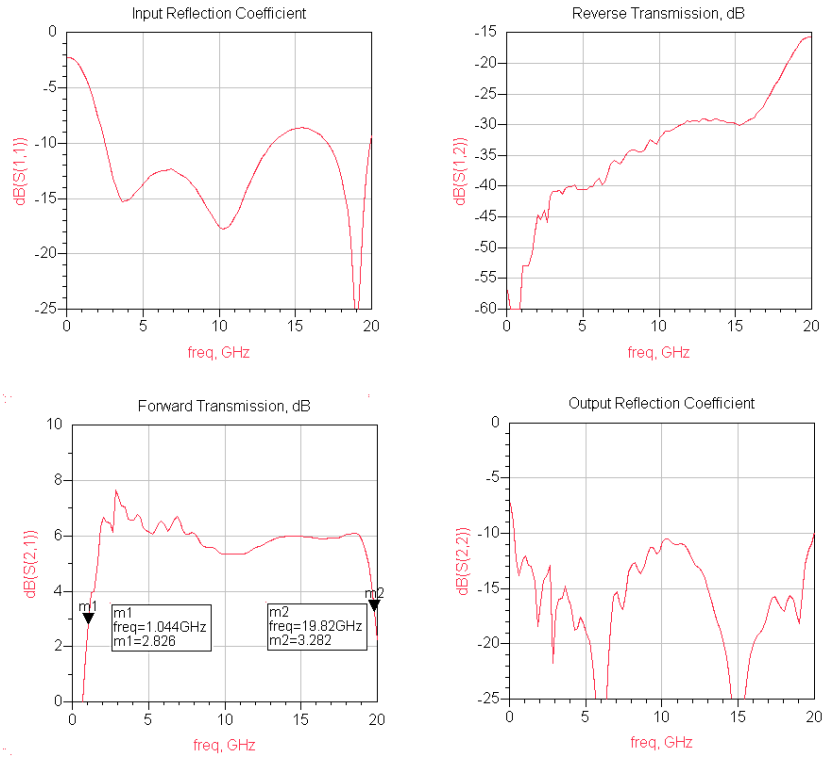


Figure 3.17 Measured S-Parameters of TWA

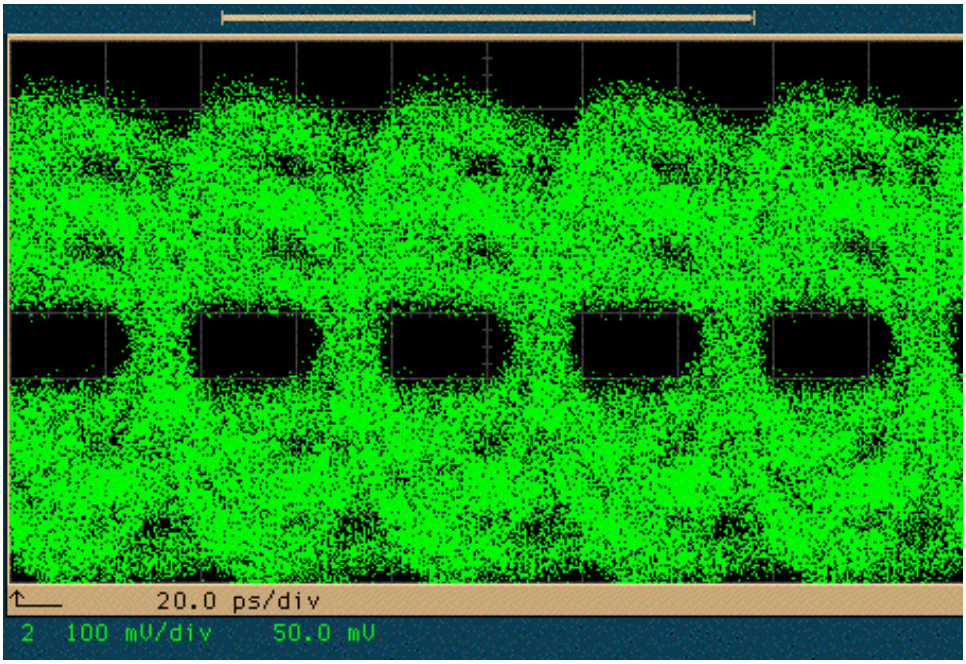


Figure 3.18 Eye diagram

CHAPTER 4

NEXT NOISE EMULATION FILTER

Background

The backplane transmission environment, including motherboard, connectors and daughter cards, is illustrated in Figure 4.1. The primary physical impediments to high data rates in legacy backplane channels are the loss characteristics of copper channels and the interference from adjacent channels. These effects become more severe as the data rate increases beyond 1 Gb/sec. Above rates of 2 Gb/sec, the skin effect and dielectric loss in copper channels of the backplane distort and severely impair signal integrity [40-43].

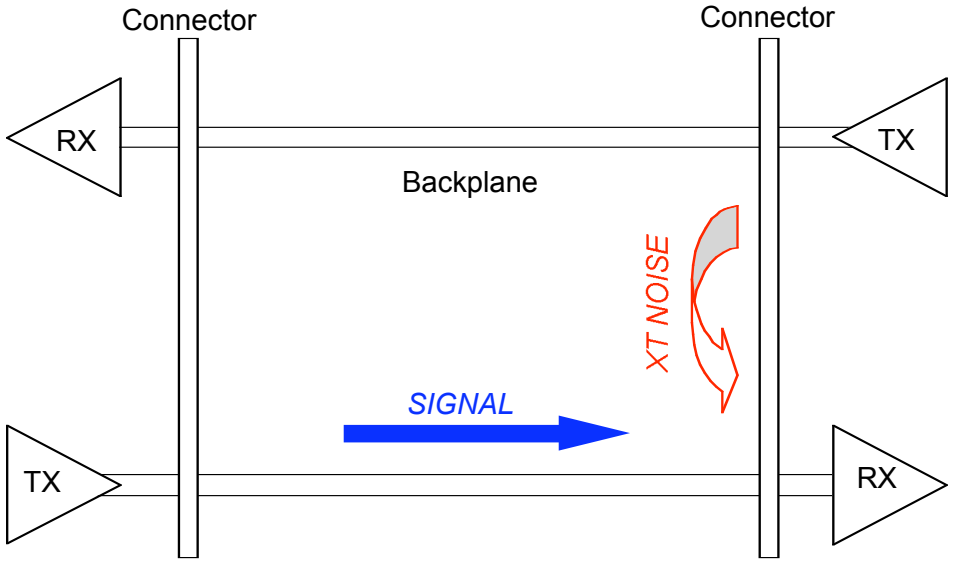


Figure 4.1 Backplane Channel Environment

The forward transmission channel of the backplane has a low-pass frequency response due to dielectric loss and skin effect [40-43], as shown in Figure 4.2. This band-limited feature induces Inter-Symbol Interference (ISI), which becomes more severe as the trace length of the backplane increases.

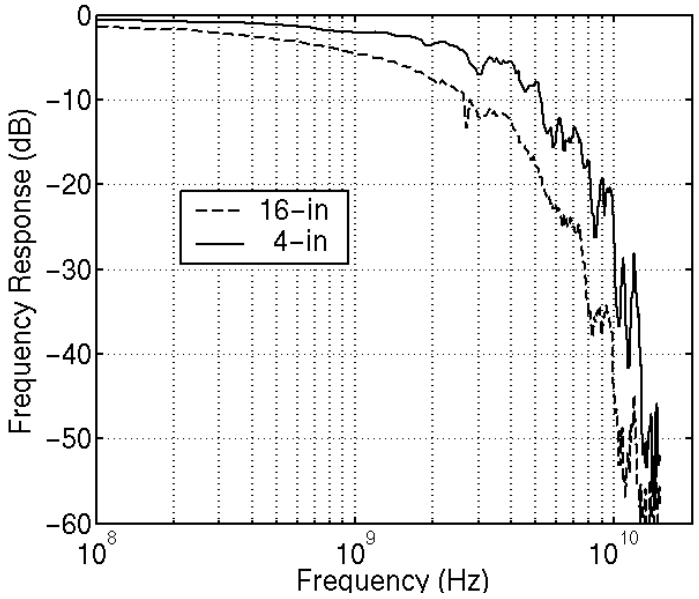


Figure 4.2 Forward Channel Characteristic of FR-4 Backplane

As the datarate, and as a direct consequence, the bandwidth, of the signal increases, unshielded pins in connectors radiate spurious signals to nearby pins. Adjacent "aggressor" channels can couple unwanted signals to contribute to noise in the "victim" channel. This noise is characterized as cross-talk (XTalk) noise and can occur at a connector close to the receiver in the channel or at a connector farther down the channel, referred to as Near-End XTalk (NEXT) and Far-End XTalk (FEXT) respectively. When

a transmitted signal passes through a backplane connector, this signal is coupled with the received signal of another transceiver resulting in data dependent XTalk noise. Because the coupled noise increases with frequency, the NEXT noise becomes the main impairment factor preventing one from achieving desired bit error rate and jitter performance above 5 Gb/sec [42-44]. NEXT noise is of a much higher magnitude than FEXT noise because of its proximity to the receiver. This NEXT noise has a high-pass frequency response, and depending on the type of connectors and backplanes, the corner frequency values and frequency response can drastically vary as shown in Figure 4.3.

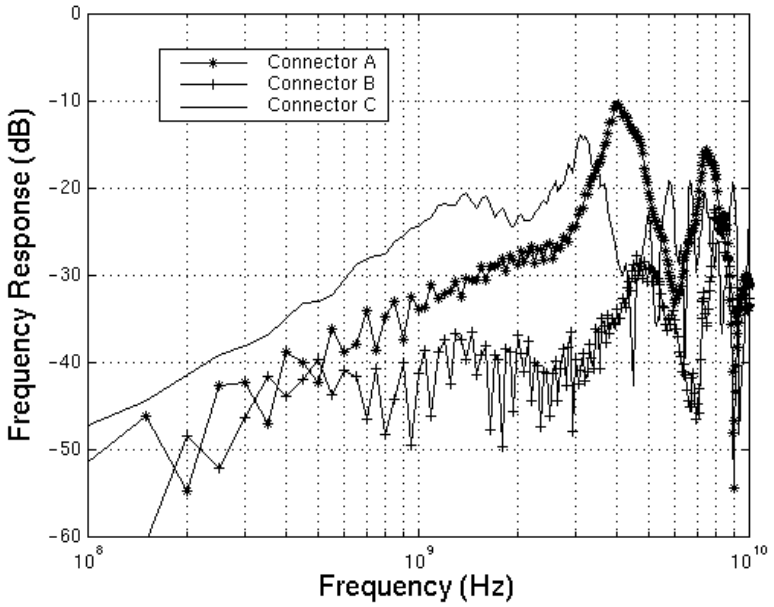


Figure 4.3 Cross Talk Channel Characteristics of Different Connectors

The channel bandwidth limitation can be addressed in several manners. These techniques include using dielectric materials with better loss characteristics, compensation of the channel induced loss via equalization techniques at the transmit and/or receiver side, and using more spectrally efficient signaling schemes [40-42], [47-

48]. To alleviate NEXT noise contributions, sophisticated connectors and active noise cancellation techniques have been proposed [45-47]. Techniques that involve drastic physical changes to the backplane environment like replacing dielectrics and connectors with improved products are difficult to implement without an invasive overhaul of the system. Less invasive techniques that can implement signal recovery by adding active circuitry onto either the transmitter or receiver can avoid complete overhaul of backplane channel. The additional circuitry is typically implemented on the daughter cards, relieving the need to replace deeply entrenched infrastructure. These less invasive techniques include equalization of the lossy channels and active cancellation of the NEXT noise. Combining these two techniques is the most efficient means to achieve high data rates.

The characteristics of the two noise sources make it critical to combine the two techniques at higher data rates. The dispersive forward channel characteristics can be alleviated by equalization techniques that boost the high frequency components of the signals [40-43]. However, because the NEXT coupling characteristic resembles a high-pass filter frequency response, applying equalization to recover the transmitted signal in the presence of NEXT will boost the high frequency components of both the received signal and NEXT noise. This effect is highlighted in Figure 4.4 where the gain of the forward channel and the NEXT channel cross each other. Therefore, the influence of NEXT noise at the higher frequencies becomes exaggerated thereby canceling any benefits from only equalization. To realize rates at 10 Gb/sec and above, it becomes imperative that XTalk noise be cancelled before equalization is applied.

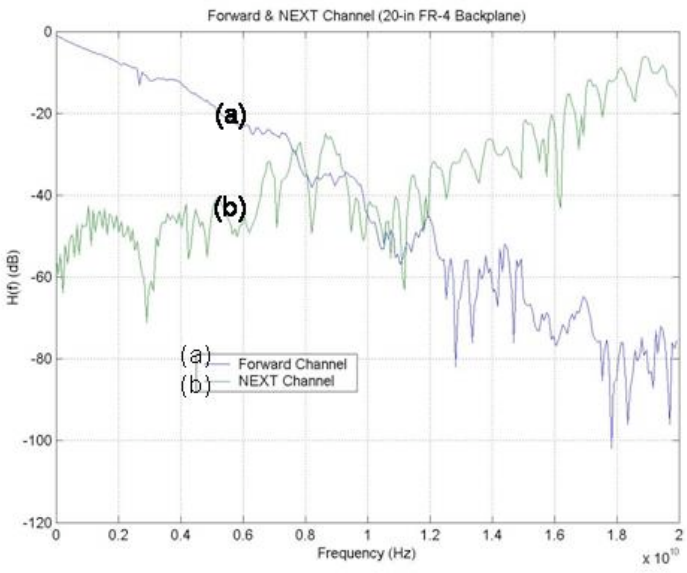


Figure 4.4 Comparison of Forward and NEXT Channel Characteristics

Figure 4.5a-d show how ISI and NEXT noise affect the signal integrity performance of a 10 Gb/sec On-Off Keying (OOK) signal. When a clean 10 Gb/sec OOK signal, as illustrated in Figure 4.5a, propagates through a 16-in backplane board trace, its eye is completely closed due to ISI, as shown in Figure 4.5b. This signal can be recovered with equalization, as depicted in Figure 4.5c. However in the presence of an aggressor, data dependent noise, i.e. NEXT noise, is coupled with the received signal before any equalization at the receiver. This NEXT noise is boosted by equalization, as shown in Figure 4.5d. Therefore, equalization must be accompanied by NEXT noise cancellation in order to obtain a complete solution for high-speed signaling at 10 Gb/sec over backplane channels.

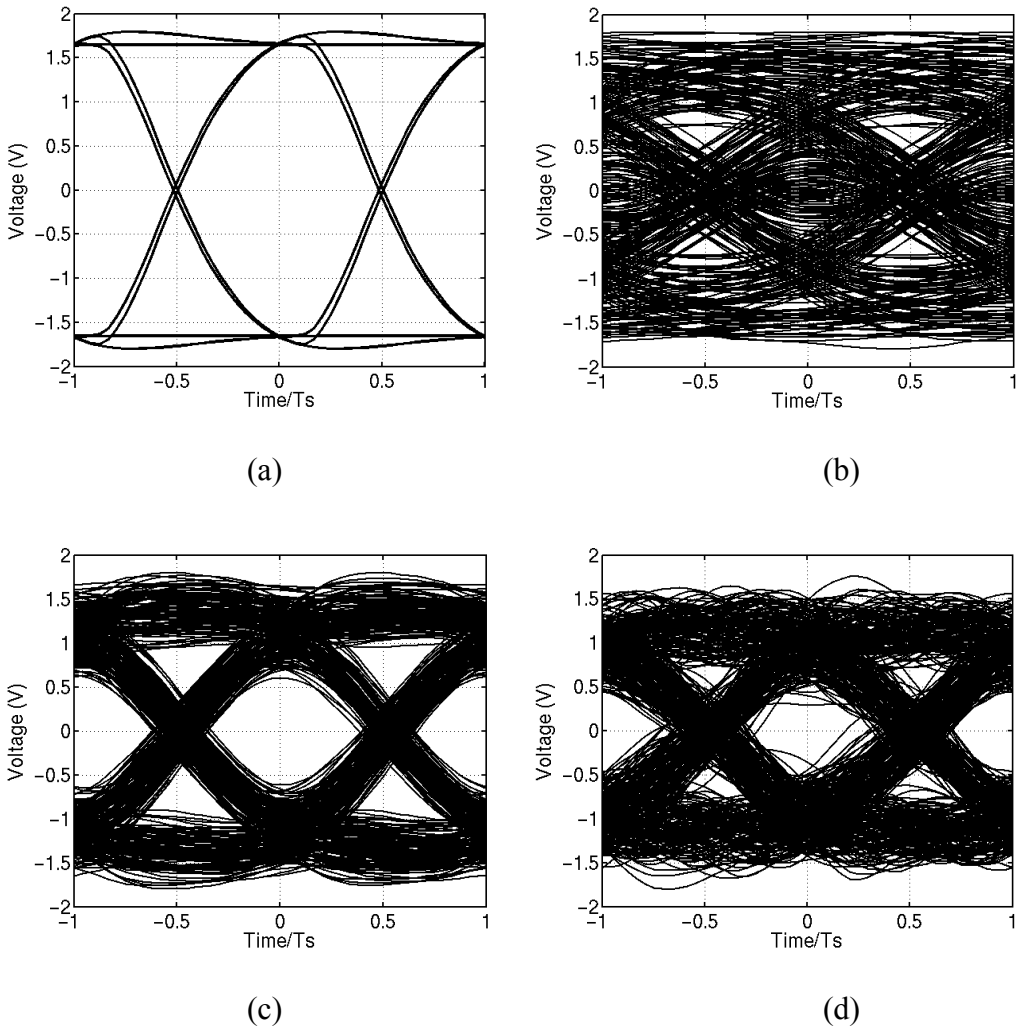


Figure 4.5 (a) 10 Gb/sec OOK Transmit Signal (b) Channel Output of 16 in FR-4 Backplane (c) Equalized Signal (d) Equalized Signal with a NEXT Aggressor Signal

In this work, a receiver side integrated CMOS solution for extending data rates into the tens of Gb/sec on legacy FR-4 backplanes is presented. An integrated solution also allows for adaptability to compensate for changes in the channel due to variations in different vendor products, differences in channel length, and environmental effects. This approach adopts a combination of 4-level Pulse Amplitude Modulation (4-PAM) signaling scheme, a CMOS Feed-Forward Equalizer (FFE) and a CMOS NEXT noise canceller to achieve 20 Gb/sec transmission over backplane channels. In this research, the coarse emulation filter for the CMOS NEXT noise canceller is discussed.

NEXT Noise Channel Cancellation Architecture

A proposed active NEXT noise canceller takes adjacent channel data and mimics the NEXT response shown in Figure 4.2 by passing the data through emulation filters. The noise canceller taps off the aggressor signal and mimics the NEXT response. This emulated NEXT noise is subtracted from the corrupted received signal to cancel out the NEXT noise generated by crosstalk in the connectors. Figure 4.6 shows the proposed architecture consisting of two stages of cancellations, a coarse and a fine cancellation, in order to distribute the complexity of a single NEXT channel emulation filter into two filters. The emulation filter is broken down into two analog filters, one for coarse cancellation and one for fine cancellation. These filters are implemented with a Pole-Zero (PZ) filter and a Finite Impulse Response (FIR) filter. These filters must be tunable to adjust to a variety of environments arising from differences in connectors and backplane configurations, as shown in Figure 4.2.

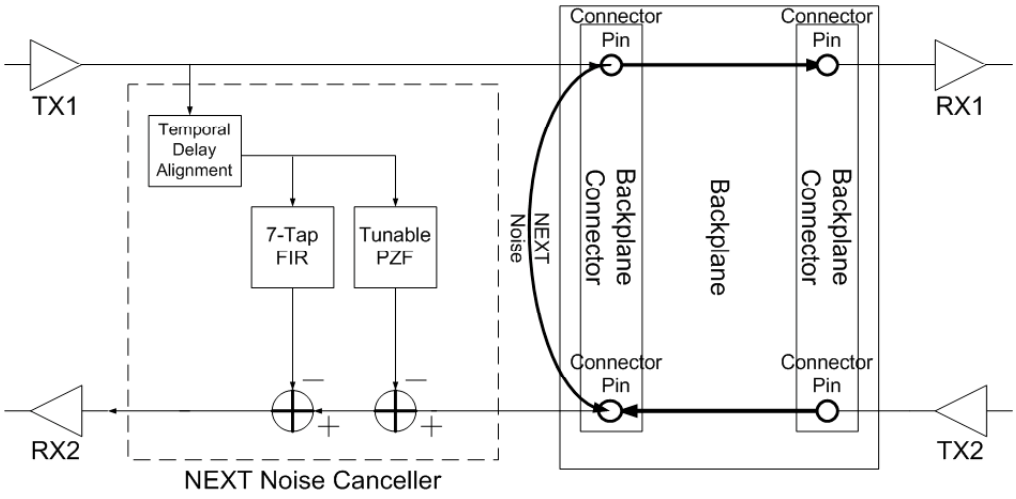


Figure 4.6 NEXT Noise Canceller Architecture

The coarse channel filter models the lower frequency components of the NEXT channel response, and the resulting emulated NEXT noise is subtracted from the received signal. In order to adapt to various types of connectors and to minimize the complexity of the FIR filter, an electrically tunable PZ filter is used so that the gain and corner frequency are adjustable.

The fine channel emulation filter matches the finer characteristic of the higher frequency components beyond the corner frequency of the coarse channel filter, and its resulting emulated NEXT noise cancels the residual NEXT noise after a coarse noise cancellation. This fine channel emulation filter has a FIR filter structure. From the system simulation results, a 7-tap Ts/3-spaced FIR filter structure is found to be optimal in terms of implementation complexity and channel emulation performance.

Another important function of the NEXT noise canceller is a temporal delay alignment, which compensates for the propagation delays induced through the daughter card trace and connectors. Because the NEXT noise is data dependent noise, the delay

alignment error increases the level of the residual NEXT noise, even when the NEXT channel emulation filters generate exactly the same waveform shape as that of actual NEXT noise.

A tunable active PZ filter circuit handles the coarse cancellation. Gain and corner frequency are adjustable to match the low frequency response of the NEXT channel. PZ filter circuit schematic is shown in Figure 4.7. Transistor M1 and M1' are connected in a common source configuration with no AC grounding between the source and the current sink. The common source configuration is a straightforward gain cell. By floating the source and not providing an AC ground or a common ground in the differential structure, the configuration has low gain at low frequencies. However, the inherent capacitance of the current sink becomes more prominent at the higher frequencies and provides a ground for the common source configuration. Lacking viable varactor structures in the CMOS process, the corner frequency is determined by the resistance of the active load. The load consists of a differential active load [49] to maintain constant DC levels at the output for different loads. Transistor M2 and M2' set the DC and common mode voltage. The static resistors and transistor M3 determine the differential load that appears at the output. Varying the bias at the gate of M3 adjusts this differential load. The bias points are not changed when the differential load is adjusted. The keeps the common mode voltage fixed going into transistors M4 and M4'. The second stage formed by transistors M4 and M4' and resistors R form the adjustable gain stage. By adjusting the current Ib2, the gain of the overall filter can be adjusted.

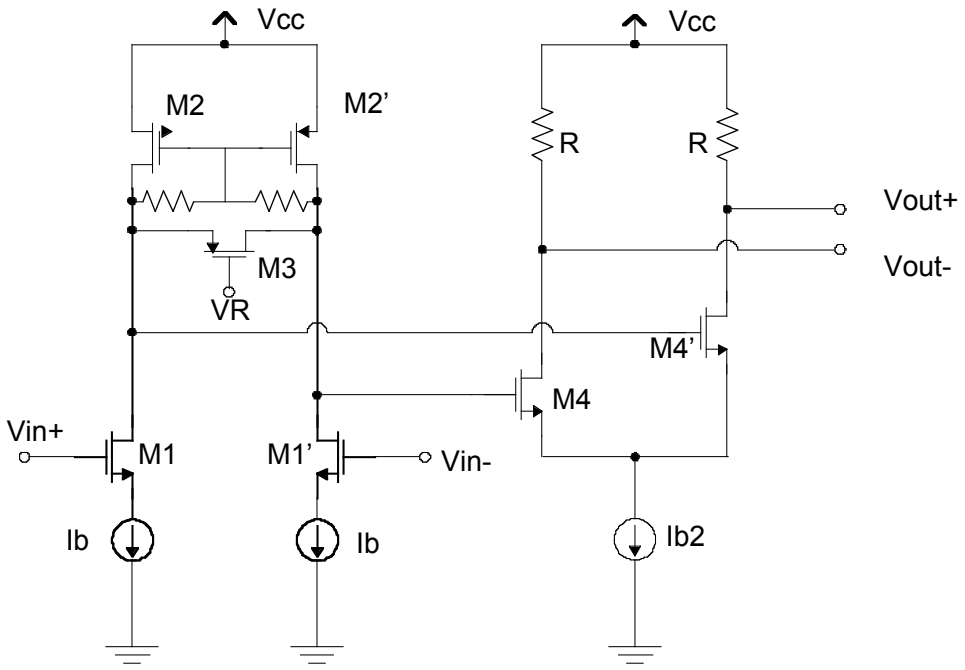


Figure 4.7 Tunable PZ Filter Schematic

PZ Filter Results

Figure 4.8 illustrates the tuning range of the proposed active tunable PZ filter. Over a 1V control signal range, the corner frequency can be adjusted from 2 GHz to over 4 GHz. Figure 4.9 demonstrates the tunable response of the PZ filter and how it can be adjusted to match the characteristics of three different channels shown in Figure 4.2 by changing its corner frequency values, i.e. 3, 4, and 4.4GHz. Figure 4.10 shows system performance of the proposed NEXT noise canceller applied to 20 Gb/sec 4-PAM signaling. Using all the sub-circuits mentioned above, the NEXT noise power is decreased by 50 % and 75 % after the coarse and fine NEXT noise cancellation, respectively. The circuit was fabricated in a 0.18 μm CMOS process to integrate with the other components of the NEXT canceller. A photograph of the circuit is shown in Figure 4.11.

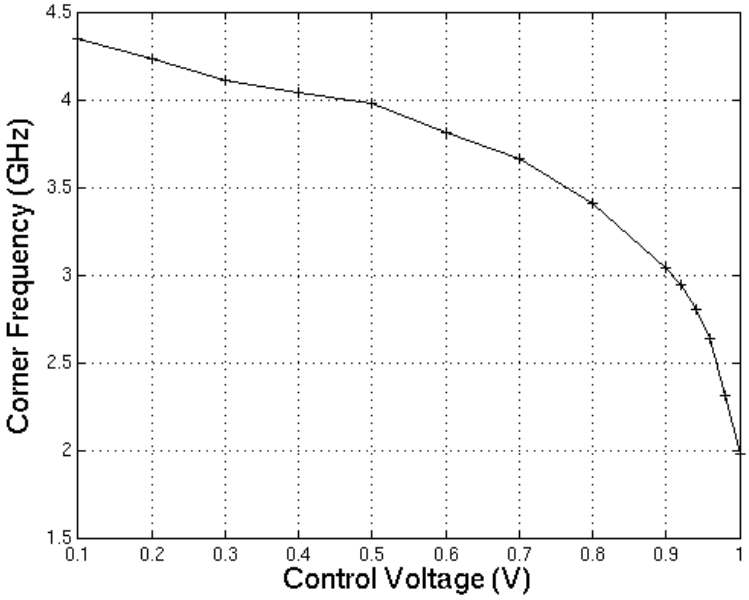


Figure 4.8 Tuning Range of PZ Corner Frequency

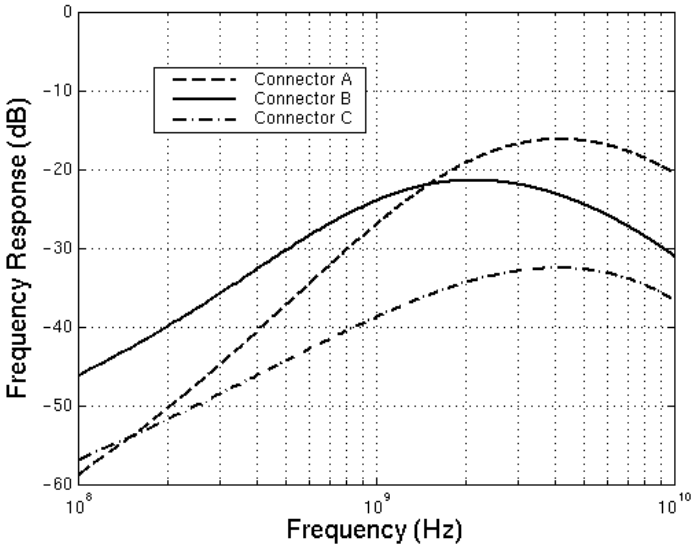


Figure 4.9 PZ Filter Emulation Response of 3 Different Connectors

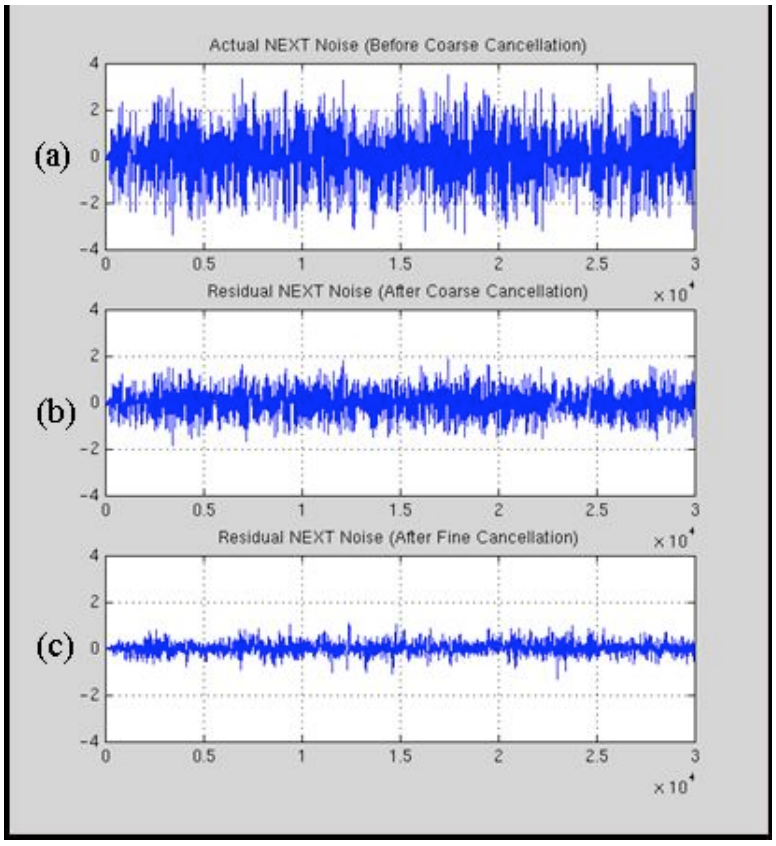


Figure 4.10 (a) NEXT Noise (b) NEXT Noise After Coarse Cancellation (c) NEXT Noise After Coarse and Fine Cancellation

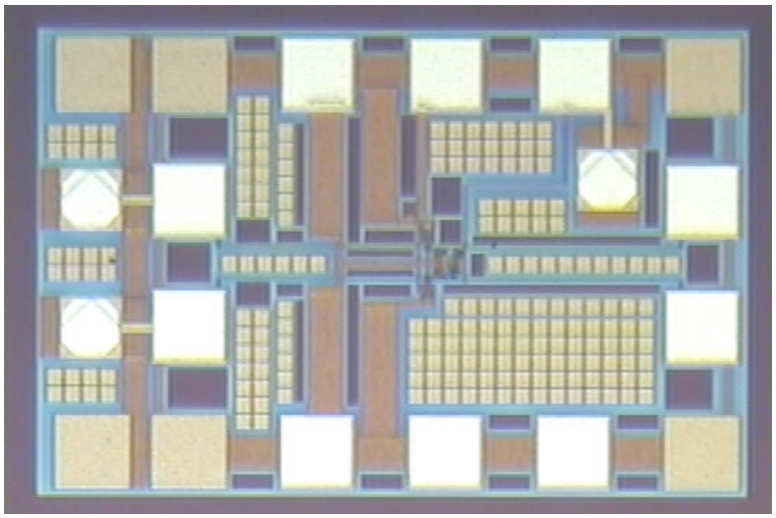


Figure 4.11 Photograph of PZ Filter

A practical solution for extending legacy backplane transmission into 20 Gb/sec operation has been presented. A combination of 4-PAM modulation and CMOS circuits that provide equalization and NEXT noise cancellation has been shown to effectively combat distortions that limit backplane performance. Tunable active filters that provide a total of 75 % NEXT noise cancellation have been presented. Experimental results from a FFE fabricated in a 0.18 um CMOS process indicate that successful data transfer is not possible without equalization. 20 Gb/sec throughput 4-PAM transmission through a 16-in backplane channel demonstrates successful operation of the equalization and NEXT noise canceller circuit.

CHAPTER 5

CONCLUSION

In this thesis, three circuits for optical based communications have been studied. The circuits are OEICs for front end receivers and noise cancellation for backplane routing. Each of the circuits was implemented in readily available commercial foundry technologies. The OEICs extend the basic functionality of the III-V process by using either parasitic photodetectors or wafer level integration of InP photodetectors. The crosstalk cancellation circuit extends legacy backplane systems by eliminating high frequency noise with a tunable CMOS filter.

The first circuit is an 8x8 monolithic receiver array for a Spatial Division Multiplexing optical link. A compact and low power 8x8 array was designed and demonstrated a channel that received data at rates of 1Gb/s. It is the first completely monolithic demonstration of a 2D receiver array within a "conventional" ion implanted GaAs MESFET process.

The second circuit demonstrated a long wavelength (1.55 μm) optoelectronic receiver for long haul applications. The circuit utilized a TWA topology, which maximizes the available bandwidth from the GaAs MESFET process. It incorporated a thin-film inverted MSM photodetector to achieve nearly monolithic integration.

The final circuit is a tunable high pass active filter in 0.18 μm CMOS technology. As part of a NEXT noise canceller architecture, it will provide the means to extend data transmission in FR-4 legacy backplanes into the tens of Gb/s datarate.

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